

99/717143  
11/23/00

# UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications  
under 37 CFR 1.53(b))

Attorney Docket No. **001545**

First Named Inventor or Application Identifier

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PAGE 2 OF 3

10. ☐ English translation Document (if applicable)

11. ☒ Information Disclosure Statement ☒ Copies of IDS Citations (PTO-1449 w/4 refs.)

12. ☐ Preliminary Amendment

13. ☒ Return Receipt Postcard (MPEP 503)

14. ☐ Small Entity Status is claimed.

☒ ☒ Claim for Convention Priority ☐ [1] Certified copy of Priority Document

a. Priority of \_\_\_\_\_ application no. \_\_\_\_\_ filed on \_\_\_\_\_ is claimed under 35 USC 119.

The certified copies/copy have/has been filed in prior application Serial No. \_\_\_\_\_.

(For Continuing Applications, if applicable).

16. ☐ Other \_\_\_\_\_

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

☐ Continuation ☐ Division ☐ Continuation-in-part (CIP) of prior application no. \_\_\_\_/\_\_\_\_

FEE TRANSMITTAL	Number Filed	Number Extra	Rate	Basic Fee
The filing fee is calculated below				\$710.00
Total Claims	8 - 20		x \$18.00	
Independent Claims	8 - 3	5	x \$80.00	400.00
Multiple Dependent Claims			\$270.00	
Basic Filing Fee				1110.00
Reduction by 1/2 for small entity				
Fee for recording enclosed Assignment			\$40.00	40.00
TOTAL				\$1150.00

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under 37 CFR 1.53(b))

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[XX] A check in the amount of \$ 1,150.00 is enclosed to cover the filing fee; including \$710.00 for filing fee; \$400.00 for 5 additional independent claims and \$40.00 for the assignment recordation fee.

[ ] Please charge our Deposit Account No. **01-2340** in the total amount of \_\_\_\_\_ to cover the filing fee and the \_\_\_\_\_ assignment recordation fee. A duplicate of this sheet is attached.

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1. The first step in the process is to identify the problem or issue that needs to be addressed. This involves gathering information and understanding the context of the problem.

2. Once the problem is identified, the next step is to define the objectives and goals of the project. This helps to clarify what needs to be achieved and provides a clear direction for the team.

3. The third step is to develop a plan or strategy to address the problem. This involves breaking down the problem into smaller, manageable tasks and determining the resources needed to complete each task.

4. The fourth step is to implement the plan. This involves putting the strategy into action and monitoring progress regularly to ensure that the project is on track.

5. The final step is to evaluate the results of the project. This involves assessing the outcomes against the objectives and goals and identifying any areas for improvement.

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Signature

Date: November 22, 2000

PTO/SB/05

INSULATED GATE TYPE SEMICONDUCTOR DEVICE AND  
METHOD FOR FABRICATING SAME

5 BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an insulated gate type semiconductor device and a method for fabricating the same, more particularly relates to an insulated gate type semiconductor device designed to prevent short-circuits, an increase in parasitic capacitance, and an increase in chip size accompanying the formation of a body contact region in a metal-oxide semiconductor field effect transistor (MOSFET) or other insulated gate type semiconductor (IGFET) using a silicon-on-insulator (SOI) substrate and a method for fabricating the same.

2. Description of the Related Art

As will be explained in detail later using the drawings, in an SOI-MOSFET using a separator, short-circuits between the body contact electrode and source and drain electrodes are prevented by the sidewalls provided at the side faces of the separator. If the sidewalls are low in height, however, in the siliciding step, silicon diffuses in the metal film deposited on the surface of the sidewalls as well and alloys the film, so the silicide at that portion cannot be removed. Therefore, there is the problem of short-circuits between the body contact electrode and source and drain electrodes through the silicide layer.

Further, when arranging the transistors in the form of an array as in the normal state of use, when adjoining separators are different in potential, it is necessary to keep the two separated by exactly a constant distance in order to prevent short-circuits between them. Due to this, there is the problem that the chip area is increased.

Further, the width of a separator is dependent on the overlay accuracy in the photolithography step at the time of formation of the separator, the variance in finishing dimensions in the etching step of the  
5 separator, the overlay accuracy of the mask at the time of ion implantation in the step of forming the body contact region, etc. Therefore, the area occupied in one transistor becomes the same order as the gate electrode functioning for forming the channel and the parasitic  
10 capacitance increases. As a result, there is the problem that the gate delay becomes greater and the performance of the device deteriorates.

#### SUMMARY OF THE INVENTION

An object of the present invention is to provide an  
15 insulated gate type semiconductor device which prevents short-circuits between electrodes, prevents short-circuits between separators, and prevents an increase of the parasitic capacitance and a method for fabricating the same.

20 To attain the above object, the present invention provides an insulated gate type semiconductor device comprised of a semiconductor layer (3) serving as an active region isolated from a semiconductor substrate (1) by a substrate isolation insulating film (2) and a T-  
25 shaped gate electrode comprised of a trunk-shaped main gate electrode (6) and a crosspiece-shaped conductor pattern (7) provided on the semiconductor layer (3), wherein the thickness of the gate insulating film directly under the crosspiece-shaped conductor pattern  
30 (7) is made greater than the thickness of the gate insulating film directly under the main gate electrode (6), whereby it is possible to prevent short-circuits between electrodes, prevent short-circuits between separators, and prevent an increase of the parasitic  
35 capacitance.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The above object and features of the present

invention will be more apparent from the following description of the preferred embodiments given with reference to the accompanying drawings, in which:

5 Fig. 1 is an explanatory view of the basic configuration of the present invention;

Fig. 2 is an explanatory view of the production process up to the middle of the first embodiment of the present invention;

10 Fig. 3 is an explanatory view of the production process up to the middle of the first embodiment of the present invention after Fig. 2;

Fig. 4 is an explanatory view of the production process up to the middle of the first embodiment of the present invention after Fig. 3;

15 Fig. 5 is an explanatory view of the production process up to the middle of the first embodiment of the present invention after Fig. 4;

20 Fig. 6 is an explanatory view of the production process up to the middle of the first embodiment of the present invention after Fig. 5;

Fig. 7 is an explanatory view of the production process up to the middle of a second embodiment of the present invention;

25 Fig. 8 is an explanatory view of the production process up to the middle of the second embodiment of the present invention after Fig. 7;

Fig. 9 is an explanatory view of the production process up to the middle of a third embodiment of the present invention;

30 Fig. 10 is an explanatory view of the production process up to the middle of the third embodiment of the present invention after Fig. 9;

35 Fig. 11 is an explanatory view of the production process up to the middle of the first embodiment of the present invention after Fig. 10;

Fig. 12 is an explanatory view of the production process up to the middle of the third embodiment of the

present invention after Fig. 11;

Fig. 13 is an explanatory view of an SOI-MOSFET according to a fourth embodiment of the present invention;

5 Fig. 14 is an explanatory view of an SOI-MOSFET according to a fifth embodiment of the present invention;

Fig. 15 is an explanatory view of a MOSFET of the related art; and

10 Fig. 16 is an explanatory view of an SOI-MOSFET of the related art.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

Before describing the embodiments of the present invention, the related art and the disadvantages therein will be described with reference to the related figures.

15 In an MOS type semiconductor device of the related art, by storing carriers in a semiconductor region where a channel region is to be formed directly under the gate electrode, the threshold voltage  $V_{th}$  and the drain current  $I_{ds}$  sometimes fluctuate and the semiconductor region enters a floating state. The above fluctuation becomes a problem in an SOI-MOS type semiconductor device, in particular a partially depleted (PD) SOI-MOS type semiconductor device with an incompletely depleted semiconductor region.

25 To prevent such fluctuations in the threshold voltage  $V_{th}$  etc., the practice in the related art had been to drain the stored carriers by forming a body contact with the semiconductor region where the channel region is to be formed. Here, an explanation will be given of a MOS type semiconductor device provided with a body contact region of the related art with reference to Fig. 15 Fig. 16.

35 Figure 15 is an explanatory view of an example of a MOSFET of the related art. Figure 15(a) is a plan view, Fig. 15(b) is a sectional view along the one-dot chain line connecting A-A' in Fig. 15(a), and Fig. 15(c) is a sectional view along the one-dot chain line connecting B-

B' in Fig. 15(a).

In this case, only an n-channel type MOSFET is shown, but in the case of a p-channel type MOSFET, the structure is substantially the same. The only difference  
5 lies in the conductivity type, i.e., the impurity used.

First, a p-type well region 72 is formed at the surface side of the p-type silicon substrate 71. An element isolation oxide film 73 surrounding the element formation region is formed using the selective oxidation  
10 (LOCOS) method or shallow trench isolation (STI) method. At the same time, an intra-element isolation oxide film 74 is formed for isolating the body contact region.

Next, a gate oxide film 75 is formed on the exposed surface of the p-type well region 72, then an electrode coating such as an amorphous silicon film is deposited  
15 over the entire surface, conductivity is imparted by ion implantation etc, then a gate electrode 76 is formed by etching. Next, phosphorus or other n-type impurity ions are implanted using the gate electrode 76 as a mask so as  
20 to form an extended diffusion region 77.

Next, an  $\text{SiO}_2$  film is deposited over the entire surface, then this is anisotropically etched to form sidewalls 78 at the side faces etc. of the gate electrode  
25 76. Next, in the state with the body contact formation region masked by a resist, phosphorus ions are implanted using the gate electrode 76 and the sidewalls 78 as a mask to form the n-type source region 79 and the n-type drain region 80.

Next, while masking the n-type source region 79 and  
30 the n-type drain region 80 by a resist, boron ions are implanted in the body contact formation region to form the body contact region 81. Next, a cobalt film is deposited over the entire surface, then heat treatment is performed to silicide it and form a silicide layer  
35 comprised of  $\text{CoSi}$  and  $\text{CoSi}_2$  on the exposed silicon region.

Next, the unreacted cobalt film is selectively



removed, then heat treatment is performed again to convert the CoSi in the silicide layer to CoSi<sub>2</sub> and form the CoSi<sub>2</sub> layers 82 to 85. This completes the basic configuration of the MOS type semiconductor device having the body contact electrode.

Note that the CoSi<sub>2</sub> layer 83 forms the source electrode, the CoSi<sub>2</sub> layer 84 forms the drain electrode, and the CoSi<sub>2</sub> layer 85 forms the body contact electrode.

Along with the higher integration degrees and higher speeds of semiconductor devices in recent years, elements have become miniaturized and the parasitic capacitance with respect to the substrate has been decreased, so attention has focused on MOS type semiconductor devices using SOI substrates with active element regions insulated and isolated from the substrate. In this type of SOI-MOS type semiconductor device, however, the active element region is completely insulated and isolated and thus brought in a floating state, so, in the case of Fig. 15, it becomes impossible to control the potential directly under the gate electrode by the body contact region through the well region.

Therefore, in the SOI-MOS type semiconductor device of the related art, it has been proposed to provide a semiconductor region having a channel formed in the gate width direction of the gate electrode (that is, the direction vertical to the longitudinal direction of the channel) and a projecting island region of the same conductivity type and provide a body contact electrode in the island region (see for example, Japanese Unexamined Patent Publication (Kokai) No. 8-125187).

Such a projecting island region for the body contact, however, is an obstacle to miniaturization of the elements, so along with the miniaturization of elements, the body contact region has been provided near the source and drain regions by using a separator and use of a silicide electrode has been experimented with to form a contact electrode by self-alignment. An SOI-MOSFET

of the related art provided with such a separator will be explained with reference to Fig. 16.

Figure 16 is an explanatory view of an example of an SOI-MOSFET of the related art. Figure 16(a) is a plan view, Fig. 16(b) is a sectional view along the one-dot chain line connecting A-A' in Fig. 16(a), and Fig. 16(c) is a sectional view along the one-dot chain line connecting B-B' in Fig. 16(a).

In this case, only an n-channel type MOSFET is shown, but even in the case of a p-channel type MOSFET, the structure is substantially the same. Only the conductivity type and therefore the impurity used differ.

First, oxygen ions are implanted to a predetermined depth in the silicon substrate 91, then heat treatment is performed to convert the oxygen ion implantation region to  $\text{SiO}_2$  to thereby form a buried oxide (BOX), that is, the substrate isolation oxide film 92. Next, boron ions are implanted in the surface to form a p-type silicon layer 93.

Next, an element isolation oxide film 94 surrounding the element formation region is formed using the STI (Shallow Trench Isolation) method, then a gate insulating film 95 is formed over the surface of the p-type silicon layer 93. Next, an amorphous silicon film or other electrode coating film is deposited over the entire surface and ions are implanted etc. to impart conductivity, then this is etched to form a T-shaped electrode pattern.

The trunk portion of the T-shaped electrode pattern forms the gate electrode 96, while the crosspiece-shaped portion thereof forms the separator 97 which has no relation to the gate operation.

Next, ions of phosphorus or another n-type impurity are implanted, using the gate electrode 96 as a mask, to thereby form an extended diffusion region 98, then an  $\text{SiO}_2$  film is deposited over the entire surface and anisotropically etched to form sidewalls 99 on the side

faces etc. of the gate electrode 96. Next, while masking the body contact formation region by a resist, phosphorus ions are implanted using the gate electrode 96, separator 97, and sidewalls 99 as a mask to form the n-type source region 100 and n-type drain region 101.

Next, while masking the n-type source region 100 and n-type drain region 101 by a resist, ions of  $\text{BF}_2$  are implanted in the body contact formation region to form the body contact region 102, then a cobalt film is deposited over the entire surface. Next, heat treatment is performed to silicide the film and form a silicide layer comprised of  $\text{CoSi}$  and  $\text{CoSi}_2$  on the exposed silicon region.

Next, the unreacted Co film is selectively removed, then heat treatment is performed again to convert the  $\text{CoSi}$  in the silicide layer to  $\text{CoSi}_2$  and thereby form the  $\text{CoSi}_2$  layers 103 to 106. This completes the basic configuration of the SOI-MOS type semiconductor device having a body contact electrode.

Note that the  $\text{CoSi}_2$  layer 104 forms the source electrode, the  $\text{CoSi}_2$  layer 105 forms the drain electrode, and the  $\text{CoSi}_2$  layer 106 forms the body contact electrode.

In such an SOI-MOSFET, the separator 97 forms part of the mask at the time of ion implantation. The electrodes of the  $\text{CoSi}_2$  layers 104 and 105 forming the source and drain electrodes and the  $\text{CoSi}_2$  layer 106 forming the body contact electrode are separated by the sidewalls 99, so the body contact electrode and the source and drain electrodes will never short-circuit.

In this case, the p-type silicon layer 93 where the channel region is to be formed is set to a predetermined potential through the body contact region 102, so fluctuation of the  $V_{th}$  is prevented. Further, the n-type source region 100 or the n-type drain region 101 contacts the body contact region 102 through the p-type silicon layer 93, so a  $p^+/n^+$  junction is never formed. Therefore, there is no fall in the drain breakdown voltage.

As already explained, in an SOI-MOSFET using a separator, short-circuits between the body contact electrode and source and drain electrodes are prevented by the sidewalls provided at the side faces of the separator. If the sidewalls are low in height, however, in the siliciding step, silicon diffuses in the metal film deposited on the surface of the sidewalls as well to alloy the film, so the silicide at that portion cannot be removed. Therefore, there is the problem of short-circuits between the body contact electrode and source and drain electrodes through the silicide layer.

Further, when arranging the transistors in the form of an array as in the normal state of use, when adjoining separators are different in potential, it is necessary to keep the two separated by exactly a constant distance in order to prevent a short-circuit between them. Due to this, there is the problem that the chip area is increased.

Further, the width of the separator is dependent on the overlay accuracy in the photolithography step at the time of formation of the separator, the variance in finishing dimensions in the etching step of the separator, the overlap accuracy of the mask at the time of ion implantation in the step of forming the body contact region, etc. Therefore, the area occupied in one transistor becomes the same order as the gate electrode functioning for forming the channel and the parasitic capacitance increases. As a result, there is the problem that the gate delay becomes greater and the performance of the device deteriorates.

Next, embodiments of the present invention for preventing short-circuits between electrodes, preventing short-circuits between separators, and preventing an increase of the parasitic capacitance will be explained in detail.

Figure 1 is an explanatory view of the basic configuration of the present invention, where Fig. 1(a)

is a plan view, Fig. 1(b) is a sectional view along the one-dot chain line connecting A-A' in Fig. 1(a), and Fig. 1(c) is a sectional view along the one-dot chain line connecting B-B' in Fig. 1(a).

5           The first aspect of the present invention comprises an insulated gate type semiconductor device comprised of a semiconductor layer 3 serving as an active region isolated from a semiconductor substrate 1 by a substrate isolation insulating film 2, provided with a T-shaped  
10 gate electrode comprised of a trunk-shaped main gate electrode 6 and a crosspiece-shaped conductor pattern 7 and having a thickness of the gate insulating film directly under the crosspiece-shaped conductor pattern 7 greater than the thickness of the gate insulating film 4  
15 directly under the main gate electrode 6.

          When providing a T-shaped gate electrode having a crosspiece-shaped conductor pattern 7, that is, a separator, in this way, the parasitic capacitance derived from the separator can be reduced by making the thickness  
20 of the gate insulating film directly under the crosspiece-shaped conductor pattern 7 greater than the thickness of the gate insulating film 4 directly below the main gate electrode 6, that is, by providing the thick portion 5.

25           Further, in the first aspect of the invention, it is preferable to provide the sidewalls 8 at the side faces of the gate electrode and provide the silicide electrode 10 at least at the exposed surface of the semiconductor layer 3.

30           That is, since the thick portion 5 of the gate insulating film 4 is directly below the separator, the thickness of the main gain electrode 6 becomes greater along with this, so the height of the sidewalls 8 becomes greater. Due to this, the silicide electrodes 10 are no  
35 longer connected with each other, so short-circuits between the silicide electrodes 10 can be prevented.

          Further, since the separation between separators of

the adjoining elements becomes more reliable due to the provision of the high sidewalls 8, an excess space for preventing short-circuits becomes unnecessary. Due to this, the pitch between transistors can be shortened.

5           The second aspect of the present invention comprises an insulated gate type semiconductor device comprised of a semiconductor layer 3 serving as an active region isolated from a semiconductor substrate 1 by a substrate isolation insulating film 2, wherein a thickness of an  
10           insulating film provided on a surface of a first conductivity type semiconductor region positioned at an interface between that first conductivity type body contact region 9 and a second conductivity type source and drain regions is made greater than the thickness of a  
15           gate insulating film 4 directly under a gate electrode.

          By making the thickness of the insulating film provided on the surface of the first conductivity type semiconductor region positioned at the interface between  
20           the first conductivity type body contact region 9 and the second conductivity type source and drain regions greater than the thickness of the gate insulating film 4 directly below the gate electrode, a separator become unnecessary, so no parasitic capacitance derived from the separator occurs. Further, no space is needed for separating  
25           separators, the pitch between transistors can be shortened accordingly.

          Further, in the second aspect of the invention, it is preferable to provide sidewalls 8 at the side faces of the gate electrode and provide a silicide electrode 10 at  
30           least at the exposed surface of the semiconductor layer 3.

          That is, since the separators of the adjoining elements are reliably insulated and separated by providing the high sidewalls 8, the excess space for  
35           isolation becomes unnecessary and there is no longer a need to consider changes in the performance of a transistor at the connecting portions of the separator

and main gate electrode 6.

Further, since a thick insulating film, that is, the thick portion 5, is provided at the surface of the first conductivity type semiconductor region positioned at the interface between the first conductivity type body contact region 9 and the second conductivity type source and drain regions, when forming the silicide electrode 10, there is no longer any risk of the surface of the first conductivity type semiconductor region positioned at the interface between the first conductivity type body contact region 9 and the second conductivity type source and drain regions becoming silicided.

The third aspect of the present invention comprises an insulated gate type semiconductor device comprised of a semiconductor layer 3 serving as an active region isolated from a semiconductor substrate 1 by a substrate isolation insulating film 2, wherein a buried insulating film thicker than the thickness of the gate insulating film 4 directly under a gate electrode is provided on a surface of a first conductivity type semiconductor region positioned at an interface between that first conductivity type body contact region 9 and a second conductivity type source and drain regions.

By providing the buried insulating film thicker than the thickness of the gate insulating film 4 directly under the gate electrode, that is, the intra-element isolation insulating film, at the surface of the first conductivity type semiconductor region positioned at the interface between the first conductivity type body contact region 9 and the second conductivity type source and drain regions, the separator becomes unnecessary, so no parasitic capacitance derived from separators occurs and there is no longer a need to consider the change in the performance of a transistor at the connecting part of the separator and main gate electrode 6.

Further, since space for separating separators from each other is no longer necessary, reduction of the pitch

between transistors becomes possible.

5 The fourth aspect of the present invention comprises  
an insulated gate type semiconductor device comprised of  
a semiconductor layer 3 serving as an active region  
isolated from a semiconductor substrate 1 by a substrate  
isolation insulating film 2, wherein a gate electrode of  
a shape of either one of an L-shape or asymmetric T-shape  
comprised of a trunk-shaped main gate electrode 6 and a  
crosspiece-shaped conductor pattern 7 is provided and a  
10 body contact region 9 and one of a source region and  
drain region are separated through the crosspiece-shaped  
conductor pattern 7.

15 In the case of an element using one of the source  
region and drain region made the same potential as the  
body contact region 9, since short-circuits between the  
separators of adjoining elements are prevented by the  
provision of a gate electrode of a shape of one of an L-  
shape or asymmetric T-shape comprised of a trunk-shaped  
main gate electrode 6 and a crosspiece-shaped conductor  
20 pattern 7, space for preventing short-circuits becomes  
unnecessary.

Further, since the length of the separator becomes  
shorter, the parasitic capacitance is also greatly  
decreased and the performance of the transistor improved.

25 The fifth aspect of the present invention comprises  
an insulated gate type semiconductor device comprised of  
a semiconductor layer 3 serving as an active region  
isolated from a semiconductor substrate 1 by a substrate  
isolation insulating film 2, wherein a gate electrode of  
a shape of either one of an L-shape or asymmetric T-shape  
comprised of a trunk-shaped main gate electrode 6 and a  
crosspiece-shaped conductor pattern 7 is provided and at  
30 least part of the crosspiece-shaped conductor pattern 7  
functions as an effective gate electrode.

35 By making at least part of the crosspiece-shaped  
conductor pattern 7 comprising the L-shaped or asymmetric  
T-shaped gate electrode an effective gate electrode, the



effective channel width is increased, so the performance of the transistor is improved.

Further, since the crosspiece-shaped conductor pattern 7 is not used as a mask at the time of forming the body contact region 9, the width of the crosspiece-shaped conductor pattern 7 can be made the same as the width of the main gate electrode 6.

Further, in the fourth and fifth aspects of the present invention, preferably provision is made of sidewalls 8 at the side faces of the gate electrode and provision is made of a silicide electrode 10 at least at the exposed surface of the semiconductor layer 3.

That is, by providing the silicide electrode 10 in this way, it is possible to integrally form the electrodes for the regions used at the same potential as the body contact region 9. On the other hand, the regions set to a different potential from the body contact region 9 can be electrically insulated by the sidewalls 8.

Further, in the first to fifth aspects of the present invention, preferably provision is made of an extended diffusion region at the semiconductor layer 3 at the side ends of the gate electrode.

That is, by providing the extended diffusion region, formation of an offset region at the side ends of the gate electrode is prevented. This is particularly effective when providing sidewalls 8.

The sixth aspect of the present invention relates to a method for fabricating an insulated gate type semiconductor device comprised of a semiconductor layer 3 serving as an active region isolated from a semiconductor substrate 1 by a substrate isolation insulating film 2, comprising the steps of providing a gate insulating film 4 partially differing in thickness on the surface of the semiconductor layer 3; providing a crosspiece-shaped conductor pattern 7 on a thick portion 5 of the gate insulating film 4 and providing a trunk-shaped main gate electrode 6 on the gate insulating film 4 to form a T-

shaped gate electrode; forming sidewalls 8 on side faces of the gate electrode; doping an impurity, using the main gate electrode 6 and crosspiece-shaped conductor pattern 7 as a mask, to form source and drain regions; doping an impurity, using the crosspiece-shaped conductor pattern 7 as a mask, to form a body contact region 9; and depositing a metal film over the entire surface then performing heat treatment to form a silicide electrode 10.

By providing the crosspiece-shaped conductor pattern 7, that is, the separator, at the thick portion 5 of the gate insulating film, it is possible to increase the height of the sidewalls 8. Due to this, it is possible to prevent a silicide electrode 10 from being formed on the sidewalls 8 and therefore possible to prevent short-circuits between silicide electrodes 10.

The seventh aspect of the present invention relates to a method for fabricating an insulated gate type semiconductor device comprised of a semiconductor layer 3 serving as an active region isolated from a semiconductor substrate 1 by a substrate isolation insulating film 2, comprising the steps of providing a gate insulating film 4 partially differing in thickness on the surface of the semiconductor layer 3; providing a crosspiece-shaped conductor pattern 7 on a thick portion 5 of the gate insulating film 4 and providing a trunk-shaped main gate electrode 6 on the gate insulating film 4 to form a T-shaped gate electrode; forming sidewalls 8 on side faces of the gate electrode; doping an impurity, using the main gate electrode 6 and crosspiece-shaped conductor pattern 7 as a mask, to form source and drain regions; doping an impurity, using the crosspiece-shaped conductor pattern 7 as a mask, to form a body contact region 9; and removing the crosspiece-shaped conductor pattern 7, then depositing a metal film over the entire surface and performing heat treatment to form a silicide electrode 10.

By removing the crosspiece-shaped pattern 7, that is, the separator, forming the mask at the time of doping of the impurity, before depositing the metal film for formation of the silicide electrode 10 over the entire surface in this way, it is possible to eliminate the parasitic capacitance due to the separator.

Further, in the siliciding step, since the thick portion 5 is present at the part from which the separator was removed, the semiconductor layer 3 will not become exposed at the washing step before the step of depositing the metal film. Therefore, the silicide electrode 10 is no longer formed at the removal part.

The eighth aspect of the present invention relates to a method for fabricating an insulated gate type semiconductor device comprised of a semiconductor layer 3 serving as an active region isolated from a semiconductor substrate 1 by a substrate isolation insulating film 2, comprising the steps of forming a groove of a different depth in the surface of the semiconductor layer 3 and burying the groove by an insulator to form an element isolation insulating film and an intra-element isolation insulating film; providing a gate electrode on a gate insulating film 4; forming sidewalls on side faces of the gate electrode; doping an impurity, using the gate electrode and the intra-element isolation insulating film as a mask, to form source and drain regions; doping an impurity, using the intra-element isolation insulating film as a mask, to form a body contact region 9; and depositing a metal film over the entire surface then performing heat treatment to form a silicide electrode 10.

By separating the body contact region 9 and the source and drain regions by the intra-element isolation insulating film comprised of the buried insulator in this way, the separator becomes unnecessary, the pitch between transistors can be shortened, and it is no longer necessary to consider the changes in the transistor

characteristics at the connecting part of the separator and the main gate electrode 6.

Further, in the sixth to eighth aspects of the present invention, there is preferably a step of doping an impurity and forming an extended diffusion region at the side ends of the gate electrode before forming the sidewalls 8.

That is, by forming the extended diffusion region before forming the sidewalls 8, it is possible to prevent the area directly under the sidewalls 8 from becoming offset regions.

Next, embodiments of the present invention will be explained.

Here, the explanation will be given of the process of production of an SOI-MOSFET according to a first embodiment of the present invention with reference to Fig. 2 to Fig. 6. To simplify the explanation, the explanation will be given of the process of production of an n-channel type MOSFET.

In Fig. 2(a), the top view is a plan view, while the bottom views are sectional views along the one-dot chain line connecting A-A' of the plan view.

First, oxygen ions are implanted to a predetermined depth in the silicon substrate 11, then heat treatment is performed to convert the oxygen ion implanted region to  $\text{SiO}_2$  and form the substrate isolation oxide film 12. Next, by implanting boron ions in the surface of the substrate, a p-type silicon layer 13 is formed.

Next, an element isolation oxide film 14 is formed around the element formation region using the STI method. Next, the surface of the p-type silicon layer 13 is heat oxidized to form the gate insulating film 15.

Next, in Fig. 2(b), the film is wet etched, using the resist pattern 16 covering the body contact formation region as a mask, so as to remove the exposed portion of the gate insulating film 15.

Next, in Fig. 3(c), the resist pattern 16 is

removed, then heat oxidation is used to form a gate insulating film 17 of a thickness of for example 4 nm.

At this time, the remainder of the gate insulating film 15 becomes a thick portion 18 of a thickness of for example 7.5 (4+3.5) nm by an extra 3.5 nm, whereby a difference in thickness is formed at the gate insulating film 17.

In Fig. 3(d), the upper view is a plan view, while the lower view is a sectional view along the one-dot chain line connecting A-A' of the plan view.

Next, an amorphous silicon film of a thickness of for example 180 nm is deposited over the entire surface, then phosphorus ions are implanted. Next, this is annealed to convert this to an n-type polycrystalline silicon film, then this film is dry etched, using the T-shaped resist pattern 19 as a mask, to form a trunk-shaped gate electrode 20 of a width of for example 0.18  $\mu\text{m}$  and a crosspiece-shaped separator 21 of a width of for example 0.50  $\mu\text{m}$ .

Next, this is wet etched to remove the exposed parts of the gate insulating film 17 and the thick portion 18 to expose the surface of the p-type silicon layer 13.

Note that in this figure, the separator 21 and the gate electrode 20 are shown by different patterns, but these are comprised by the same n-type polycrystalline silicon film.

In Fig. 4(e), the top view is a plan view, the middle view is a sectional view along the one-dot chain line connecting A-A' of the plan view, and the bottom view is a sectional view along the one-dot chain line connecting B-B' of the plan view.

Next, the body contact formation region is covered by a resist pattern (not shown), then phosphorus ions are implanted. Due to this, an n-type extended diffusion region 27 is formed directly under the side ends of the gate electrode 20.

Next, an  $\text{SiO}_2$  film is deposited over the entire surface, then this is anisotropically etched to form sidewalls 22 on the side faces of the gate electrode 20 and the separator 21. Next, while masking the body contact formation region by the resist pattern 23, phosphorus ions 24 are implanted using the gate electrode 20, separator 21, and sidewalls 22 as a mask to form the n-type source region 25 and n-type drain region 26.

Next, in Fig. 5(f), the resist pattern 23 is removed. Then, while masking the n-type source region 25 and the n-type drain region 26 by the resist pattern 28, boron ions 29 are implanted to form the body contact region 30.

In Fig. 5(g), the top view is a sectional view along A-A', while the bottom view is a sectional view along B-B'.

Next, the resist pattern 28 is removed, then the remainder is washed. Next, a cobalt film 31 is deposited over the entire surface using the sputtering method.

In Fig. 6(h), the top view is a plan view, the middle view is a sectional view along the one-dot chain line connecting A-A' of the plan view, and the bottom view is a sectional view along the one-dot chain line connecting B-B' of the plan view.

Next, rapid thermal annealing (RTA) is performed in an  $\text{N}_2$  atmosphere to cause a reaction between the cobalt film 31 and silicon and form a CoSi layer. Next, this is etched using a mixture of  $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2 = 3:1$  to remove the unreacted cobalt film on the insulating films of the element isolation oxide film 14, sidewalls 22, and so on.

Next, RTA is performed again in an  $\text{N}_2$  atmosphere to cause a reaction again between the CoSi layer and silicon to form  $\text{CoSi}_2$  layers 32 of low resistance on each surface of the gate electrode 20, separator 21, n-type source region 25, n-type drain region 26, and body contact region 30. This completes the basic structure of the SOI-MOSFET.

In this case, the height of the sidewalls 22 formed on the side faces of the separator 21 becomes greater due to the presence of the thick portion 18, so at the time of the siliciding reaction, the cobalt film 31 on the surface of the sidewalls 22 will not become silicided. Therefore, the separators 21 of the adjoining elements are never electrically connected through the silicide layer formed on the sidewalls 22. As a result, the pitch between elements can be shortened.

Further, since the separator 21 is made a thickness of an extent acting as a mask at the time of ion implantation, the thickness of the gate electrode 20 also becomes thicker as a result. Therefore, the sidewalls 22 of the side faces of the gate electrode 20 also become higher, so short-circuits between  $\text{CoSi}_2$  layers 32 can also be prevented.

Further, since the thick portion 18 is present directly below the separator 21, the parasitic capacitance derived from the separator 21 can be reduced by a great degree. Due to this, the gate delay can also be reduced.

Note that the two-step process for forming the thick portion 18 does not result in an increase in the number of steps since it forms the same process as that for forming the high breakdown voltage transistors comprising the peripheral circuits.

Next, an explanation will be made of the process of production of an SOI-MOSFET according to a second embodiment of the present invention with reference to Fig. 7 and Fig. 8.

First, in Fig. 7(a), in exactly the same way as the first embodiment, the steps until Fig. 5(f) are carried out to form the body contact region 30, then the resist pattern 28 is removed to obtain the structure of Fig. 7(a).

Next, in Fig. 7(b), this is dry etched, using the resist pattern 33 having an opening of a shape

corresponding to the separator 21 as a mask, to thereby selectively remove only the separator 21.

Next, in Fig. 7(c), the resist pattern 33 is removed, then the remainder is washed. Next, a cobalt film 31 is deposited over the entire surface using the sputtering method.

In the washing step, since the thick portion 18 is present at the removed part of the separator 21, the  $\text{SiO}_2$  film at the removed part will not be removed by etching to expose the p-type silicon layer. Therefore, in that portion, the p-type silicon layer 13 and the cobalt film 31 will never come into contact.

In Fig. 8(d), the top view is a plan view, the middle view is a sectional view along the one-dot chain line connecting A-A' of the plan view, and the bottom view is a sectional view along the one-dot chain line connecting B-B' of the plan view.

Next, RTA is performed in an  $\text{N}_2$  atmosphere to cause a reaction between the cobalt film 31 and the silicon and form a  $\text{CoSi}$  layer. Next, etching is performed using a mixture of  $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2 = 3:1$  to remove the unreacted cobalt film on the insulating films such as the element isolation oxide film 14, thick portion 18, and sidewalls 22.

Next, RTA is performed again in an  $\text{N}_2$  atmosphere to cause a reaction again between the  $\text{CoSi}$  layer and silicon to form  $\text{CoSi}_2$  layers 32 of low resistance on each surface of the gate electrode 20, n-type source region 25, n-type drain region 26, and body contact region 30. This completes the basic structure of the SOI-MOSFET.

In the second embodiment, since the separator 21 used as a mask at the time of ion implantation is removed after ion implantation, the parasitic capacitance derived from the separator 21 can be eliminated. As a result, there is no longer any gate delay derived from the separator 21.

Further, in the siliciding step, even if there are a



large number of  $\text{CoSi}_2$  layers 32 formed projecting from the ends of gate electrode 20 in the direction of gate width, the parasitic capacitance does not become a problem since the layers are on the thick portion 18.

5 Further, since the separator 21 is removed, there is no longer any connecting portion between the gate electrode 20 and separator 21. Therefore, there is no longer any need to consider changes in the transistor characteristics due to such connecting portion.

10 Next, an explanation will be given of the process of production of an SOI-MOSFET of the third embodiment of the present invention with reference to Fig. 9 to Fig. 12.

15 First, in Fig. 9(a), oxygen ions are implanted to a predetermined depth in the silicon substrate 11, the heat treatment is performed to convert the oxygen ion implantation region to  $\text{SiO}_2$  and thereby form the substrate isolation oxide film 12. Next, boron ions are implanted in the surface to form the p-type silicon layer 41. Next, the underlying  $\text{SiO}_2$  film 42 and the  $\text{SiN}$  film 43 serving as the stopper in the chemical mechanical polishing (CMP) step are successively formed.

20 Next, in Fig. 9(b), this is dry etched, using the resist pattern 44 as a mask, to thereby form a shallow trench 45 for separating the body contact formation region and the other regions.

25 Next, in Fig. 9(c), the resist pattern 44 is removed, then the remainder is dry etched, using a newly provided resist pattern 46 as a mask, to form an element isolation trench 47 having a depth reaching the substrate isolation oxide film 12 surrounding the element formation region.

30 Next, in Fig. 10(d), an  $\text{SiO}_2$  film 48 is deposited over the entire surface using the high density plasma (HDP) CVD method so as to completely bury the shallow trench 45 and the element isolation trench 47 by the  $\text{SiO}_2$  film 48.

Next, in Fig. 10(e), the  $\text{SiO}_2$  film 48 is polished by the CMP method to remove the  $\text{SiO}_2$  film 48 until the  $\text{SiN}$  film 43 is exposed. Due to this, the element isolation oxide film 49 burying the element isolation trench 47 and intra-element isolation oxide film 50 burying the shallow trench 45 are formed.

Next, in Fig. 10(f), the  $\text{SiN}$  film 43 and the  $\text{SiO}_2$  film 42 are removed, then boron ions 51 are implanted in the entire surface to convert the silicon layer 41 to a p-type silicon layer 52.

Next, in Fig. 11(g), the gate insulating film 53 comprised of the  $\text{SiON}$  film is formed on the surface of the element formation region.

In Fig. 11(h), the upper view is a plan view, while the lower view is a sectional view along the one-dot chain line connecting A-A' of the plan view.

Next, an amorphous silicon film of a thickness of for example 180 nm is deposited over the entire surface, then phosphorus ions are implanted. Next, this is annealed to convert this to an n-type polycrystalline silicon film, then this film is dry etched to form a gate electrode 54 of a width of for example 0.18  $\mu\text{m}$ .

Next, this is wet etched to remove the exposed parts of the gate insulating film 53 and expose the surface of the p-type silicon layer 52.

In Fig. 12(i), the top view is a plan view, the middle view is a sectional view along the one-dot chain line connecting A-A' of the plan view, and the bottom view is a sectional view along the one-dot chain line connecting B-B' of the plan view.

Next, the body contact formation region is covered by a resist pattern, then phosphorus ions are implanted. Due to this, an n-type extended diffusion region 56 is formed.

Next, an  $\text{SiO}_2$  film is deposited over the entire surface, then this is anisotropically etched to form sidewalls 55 on the side faces of the gate electrode 54.

Next, while masking the body contact formation region by the resist pattern, phosphorus ions are implanted, using the gate electrode 54 and sidewalls 55 as a mask, to form the n-type source region 57 and n-type drain region 58.

5       Next, the resist pattern is removed, then in the state with the n-type source region 57 and the n-type drain region 58 masked by the resist pattern, boron ions are implanted to form the body contact region 30.

10       After this, exactly the same process is followed as in the first embodiment so as to form the  $\text{CoSi}_2$  layers 32 of low resistance on the surfaces of the gate electrode 54, n-type source region 57, n-type drain region 58, and body contact region 30. This completes the basic structure of the SOI-MOSFET.

15       In the third embodiment, the intra-element isolation oxide film 50 for isolating the body contact formation region is formed beforehand and the thickness of the intra-element isolation oxide film 50 is made one of at least  $0.08 \mu\text{m}$  which substantially prevents the doping of an impurity, so the separator becomes unnecessary.  
20       Therefore, in the same way as the above second embodiment, it is possible to eliminate the parasitic capacitance derived from the separator. Further, it is possible to reduce the pitch between elements.

25       Next, an explanation will be given of an SOI-MOSFET according to a fourth embodiment of the present invention with reference to Fig. 13. The process of production itself is similar to that of the first embodiment except for not forming the thick portion at the gate insulating film, so the explanation thereof will be omitted.  
30

      Figure 13(a) is a plan view, Fig. 13(b) is a sectional view along the one-dot chain line connecting A-A' in Fig. 13(a), and Fig. 13(c) is a sectional view along the one-dot chain line connecting B-B' in Fig. 13(a). Referring to Figs. 13(a) to 13(c), the SOI-MOSFET according to the fourth embodiment has a separator 61  
35       provided at only the n-type drain region 26 side.

Therefore, the p-type body contact region 30 and n-type source region 25 are short-circuited, as a whole, by the  $\text{CoSi}_2$  layer 64.

That is, in the normal circuit configuration, the source region and the substrate region where the channel is formed are sometimes used at the same potential. The above structure is used in this case. The substrate region, that is, the p-type silicon layer 13, is set to substantially the same potential as the n-type source region 25 through the body contact region 30.

In the fourth embodiment, the separator 61 becomes short, so the parasitic capacitance derived from the separator 61 can be reduced to a great extent. Due to this, the transistor characteristics can be improved.

Further, the area at the side where the separator 61 is removed is reduced.

Next, an explanation will be given of an SOI-MOSFET according to a fifth embodiment of the present invention with reference to Fig. 14. The process of production itself has many points in common with the first embodiment, so mainly the points of difference will be explained.

Figure 14(a) is a plan view, Fig. 14(b) is a sectional view along the one-dot chain line connecting A-A' in Fig. 14(a), and Fig. 14(c) is a sectional view along the one-dot chain line connecting B-B' in Fig. 14(a).

Referring to Figs. 14(a) to 14(c), the SOI-MOSFET according to the fifth embodiment has a gate electrode 20 projected out somewhat toward the body contact formation region side when patterning the n-type polysilicon layer and has the separator 65 provided at only the drain region formation side.

The resist pattern is provided so that the area near the body contact formation region side of the separator 65 is exposed when forming the source and drain regions. By implanting phosphorus ions using this resist pattern

as a mask, an n-type drain region 26 is formed and further an n-type source region 25 is formed as well at both the body contact formation region side of the separator 65 and the region where the separator 65 is not provided.

Next, a resist pattern is provided covering the n-type source region 25 and the n-type drain region 26. By implanting boron ions using the resist pattern as a mask, a body contact region 30 is formed.

After this, a silicide formation step similar to that of the first embodiment is used to form the  $\text{CoSi}_2$  layers 62 to 64. This completes the basic configuration of the SOI-MOSFET of the fifth embodiment of the present invention.

Note that in this case as well, the p-type body contact region 30 and the n-type source region 25 are short-circuited, as a whole, by the  $\text{CoSi}_2$  layer 64.

In the fifth embodiment, since the separator 65 functions effectively as a gate electrode, the effective gate width can be lengthened by the amount of the length of the separator 65. Due to this, the transistor characteristics can be improved.

Further, the width of the separator 65 in this case has to be made the same as the width of the gate electrode 20 so as to ensure uniform operating characteristics of the transistors. Along with this, the gate capacitance derived from the separators 65 can be reduced.

While the invention has been described with reference to specific embodiment chosen for purpose of illustration, it should be apparent that numerous modifications could be made thereto by those skilled in the art without departing from the basic concept and scope of the invention.

For example, in the embodiments of the present invention, the SOI structure was formed by the separation-by-implanted-oxygen (SIOX) method, but the

substrate bonding method may also be used.

For example, an  $\text{SiO}_2$  film is formed on the surface of a monocrystalline silicon substrate, then the bonding substrate comprised of a monocrystalline silicon  
5 substrate is bonded to the surface of the  $\text{SiO}_2$  film.  
Next, this is ground or ordinarily polished to remove the majority of the monocrystalline silicon substrate.  
Further, the surface is given a mirror finish to thereby provide an element formation layer insulated and isolated  
10 from the bonding substrate by the  $\text{SiO}_2$  film.

Further, in the above embodiments, the element isolation insulating film was formed by the STI method, but the invention is not limited to the STI method. The LOCOS method etc. may also be used. Further, the element  
15 isolation insulating film may also be formed before forming the BOX (Buried Oxide).

In particular, in the case of use of the substrate bonding method, element isolation grooves are formed in the monocrystalline silicon substrate, then a CVD- $\text{SiO}_2$   
20 film is deposited over the entire surface by the CVD method to bury the element isolation grooves and flatten the surface. Next, the bonding substrate comprised of the monocrystalline silicon substrate is bonded to the surface of the CVD- $\text{SiO}_2$  film, then this is ground or  
25 normally polished to remove the majority of the monocrystalline silicon substrate and give the surface a mirror finish. Due to this, an SOI substrate provided with an element isolation insulating film may be formed.

Further, in the above first, second, fourth, and  
30 fifth embodiments, an  $\text{SiO}_2$  film formed by thermal oxidation was used as the gate insulating film, but a CVD film is also possible. Further, the invention is not limited to such an  $\text{SiO}_2$  film. It is also possible to use an SiON film in the same way as in the above third  
35 embodiment. Conversely, in the third embodiment, it is also possible to use an  $\text{SiO}_2$  film as the gate insulating film.

Further, in the above embodiments, an extended diffusion region was provided, but this is not necessarily required. Instead of such an extended diffusion region, an n-type lightly doped drain (LDD) region may also be formed.

Further, in the above embodiments, a  $\text{CoSi}_2$  layer was formed using a Co film when forming the silicide electrode, but the invention is not limited to such a  $\text{CoSi}_2$  layer. It is also possible to use a Ti film and use a  $\text{TiSi}_2$  layer as the silicide electrode.

Further, in the above embodiments, the explanation was simplified by using an n-channel type MOSFET as an example, but the invention may be similarly applied to a p-channel type MOSFET. In particular, it is also possible to provide adjointingly a p-channel type MOSFET and n-channel type MOSFET separated by an element isolation insulating film and commonly connect the gate electrodes to form a known inverter.

According to the present invention, it is possible to reduce or eliminate the parasitic capacitance derived from the separators and possible to prevent short-circuits between silicide electrodes. Due to this, it becomes possible to prevent short-circuits between the body contact electrode and drain electrode and short-circuits between adjoining separators and possible to reduce the pitch between transistors. This contributes a great deal to the higher degree of integration and faster speed of insulated gate type integrated semiconductor devices.

What is claimed is

1. An insulated gate type semiconductor device  
comprised of a semiconductor layer serving as an active  
region isolated from a semiconductor substrate by a  
5 substrate isolation insulating film, provided with a T-  
shaped gate electrode comprised of a trunk-shaped main  
gate electrode and a crosspiece-shaped conductor pattern  
and having a thickness of the gate insulating film  
10 directly under the crosspiece-shaped conductor pattern  
greater than the thickness of the gate insulating film  
directly under the main gate electrode.

2. An insulated gate type semiconductor device  
comprised of a semiconductor layer serving as an active  
region isolated from a semiconductor substrate by a  
15 substrate isolation insulating film, wherein a thickness  
of an insulating film provided on a surface of a first  
conductivity type semiconductor region positioned at an  
interface between that first conductivity type body  
contact region and a second conductivity type source and  
20 drain regions is made greater than the thickness of a  
gate insulating film directly under a gate electrode.

3. An insulated gate type semiconductor device  
comprised of a semiconductor layer serving as an active  
region isolated from a semiconductor substrate by a  
25 substrate isolation insulating film, wherein a buried  
insulating film thicker than the thickness of the gate  
insulating film directly under a gate electrode is  
provided on a surface of a first conductivity type  
semiconductor region positioned at an interface between  
30 that first conductivity type body contact region and a  
second conductivity type source and drain regions.

4. An insulated gate type semiconductor device  
comprised of a semiconductor layer serving as an active  
region isolated from a semiconductor substrate by a  
35 substrate isolation insulating film, wherein a gate  
electrode of a shape of either one of an L-shape or  
asymmetric T-shape comprised of a trunk-shaped main gate



electrode and a crosspiece-shaped conductor pattern is provided and a body contact region and one of a source region and drain region are isolated through said crosspiece-shaped conductor pattern.

5           5.    An insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate by a substrate isolation insulating film, wherein a gate electrode of a shape of either one of an L-shape or  
10   asymmetric T-shape comprised of a trunk-shaped main gate electrode and a crosspiece-shaped conductor pattern is provided and at least part of said crosspiece-shaped conductor pattern functions as an effective gate electrode.

15           6.    A method for fabricating an insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate by a substrate isolation insulating film, comprising the steps of:

20                   providing a gate insulating film partially differing in thickness on the surface of said semiconductor layer;

                  providing a crosspiece-shaped conductor pattern on a thick portion of said gate insulating film and providing a trunk-shaped main gate electrode on the  
25   gate insulating film to form a T-shaped gate electrode;

                  forming sidewalls on side faces of said gate electrode;

30                   doping an impurity using said main gate electrode and crosspiece-shaped conductor pattern as a mask to form source and drain regions;

                  doping an impurity using said crosspiece-shaped conductor pattern as a mask to form a body contact region; and

35                   depositing a metal film over the entire surface and then performing heat treatment to form a silicide electrode.

7. A method for fabricating an insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate by a substrate isolation insulating film, comprising the steps of:

providing a gate insulating film partially differing in thickness on the surface of said semiconductor layer;

providing a crosspiece-shaped conductor pattern on a thick portion of said gate insulating film and providing a trunk-shaped main gate electrode on the gate insulating film to form a T-shaped gate electrode;

forming sidewalls on side faces of said gate electrode;

doping an impurity using said main gate electrode and crosspiece-shaped conductor pattern as a mask to form source and drain regions;

doping an impurity using said crosspiece-shaped conductor pattern as a mask to form a body contact region; and

removing said crosspiece-shaped conductor pattern, then depositing a metal film over the entire surface and performing heat treatment to form a silicide electrode.

8. A method for fabricating an insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate by a substrate isolation insulating film, comprising the steps of:

forming a groove of a different depth in the surface of said semiconductor layer and burying the groove by an insulator to form an element isolation insulating film and an intra-element isolation insulating film;

providing a gate electrode on a gate insulating film;

forming sidewalls on side faces of said

gate electrode;

doping an impurity using said gate  
electrode and said intra-element isolation insulating  
film as a mask to form source and drain regions;

5               doping an impurity using said intra-  
element isolation insulating film as a mask to form a  
body contact region; and

              depositing a metal film over the entire  
surface and then performing heat treatment to form a  
10           silicide electrode.

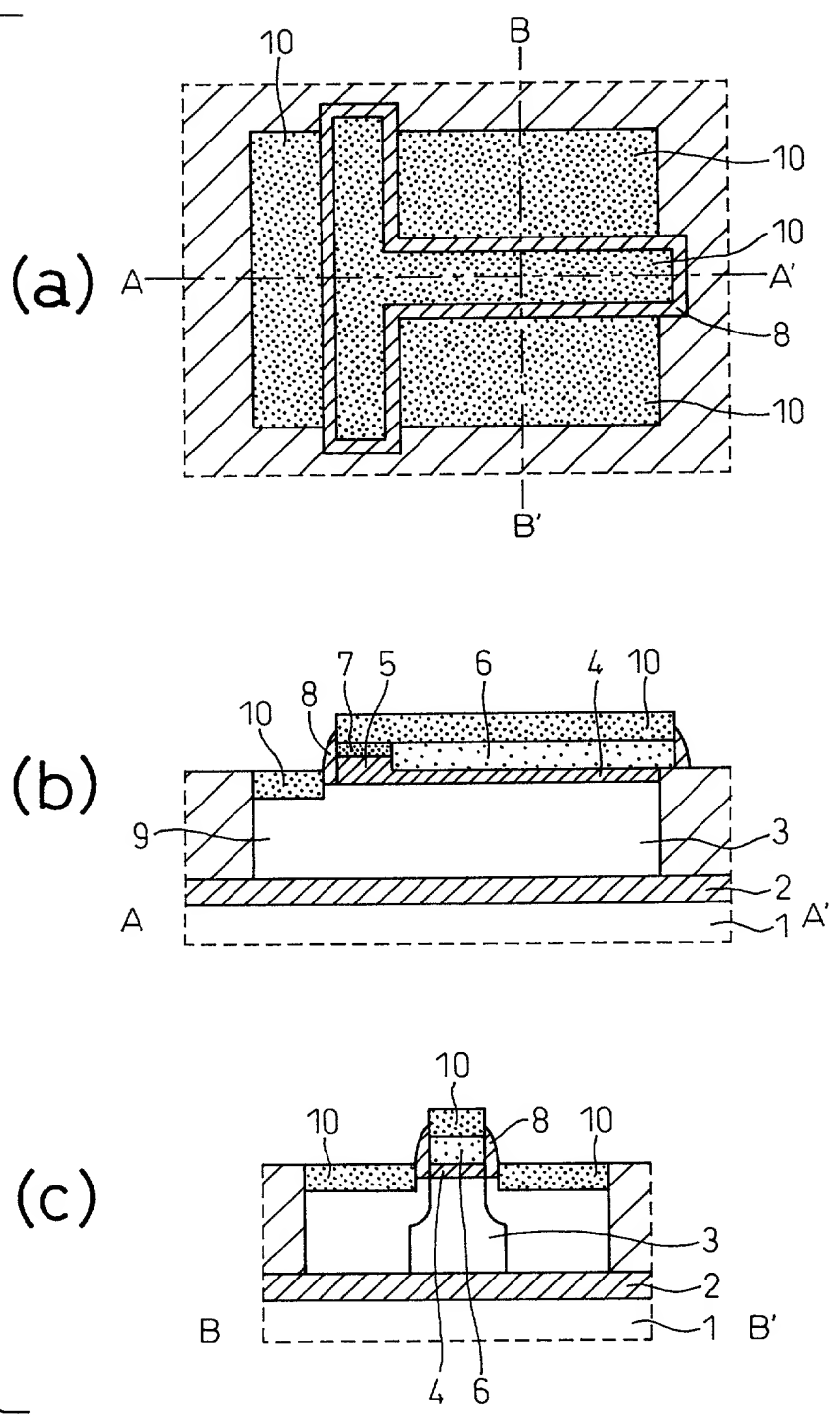
INSULATED GATE TYPE SEMICONDUCTOR DEVICE AND  
METHOD FOR FABRICATING SAME

5

ABSTRACT OF THE DISCLOSURE

10 An insulated gate type semiconductor device  
comprised of a semiconductor layer serving as an active  
region isolated from a semiconductor substrate by a  
substrate isolation insulating film and a T-shaped gate  
electrode comprised of a trunk-shaped main gate electrode  
and a crosspiece-shaped conductor pattern provided on the  
15 semiconductor layer, wherein the thickness of the gate  
insulating film directly under the crosspiece-shaped  
conductor pattern is made greater than the thickness of  
the gate insulating film directly under the main gate  
electrode, whereby it is possible to prevent short-  
20 circuits between electrodes, prevent short-circuits  
between separators, and prevent an increase of the  
parasitic capacitance.

Fig.1



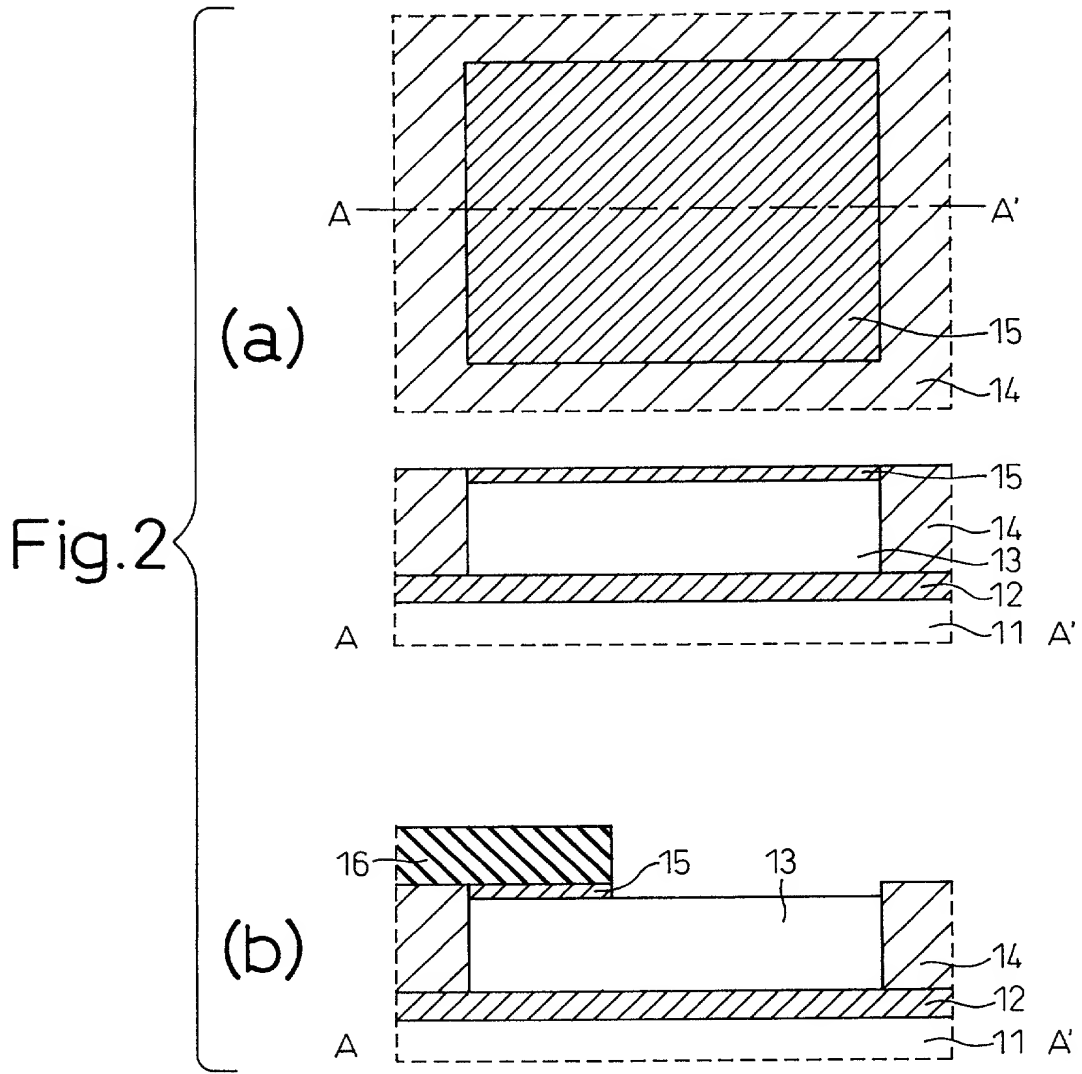
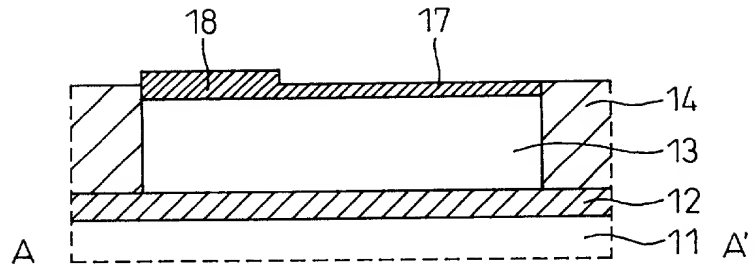


Fig.3

(c)



(d)

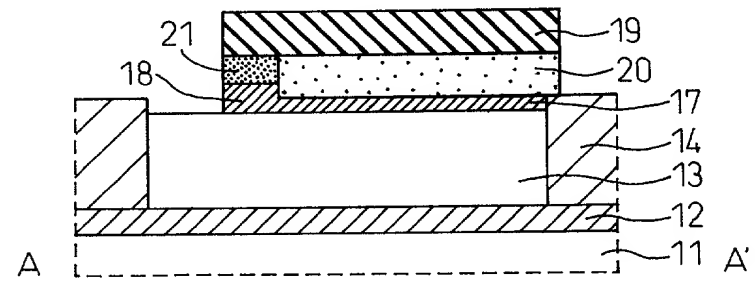
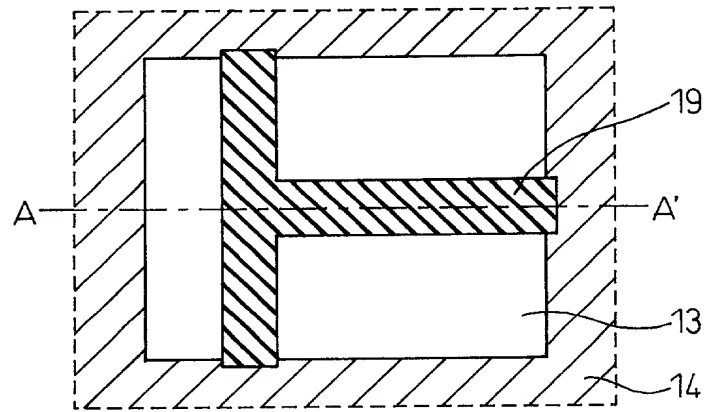
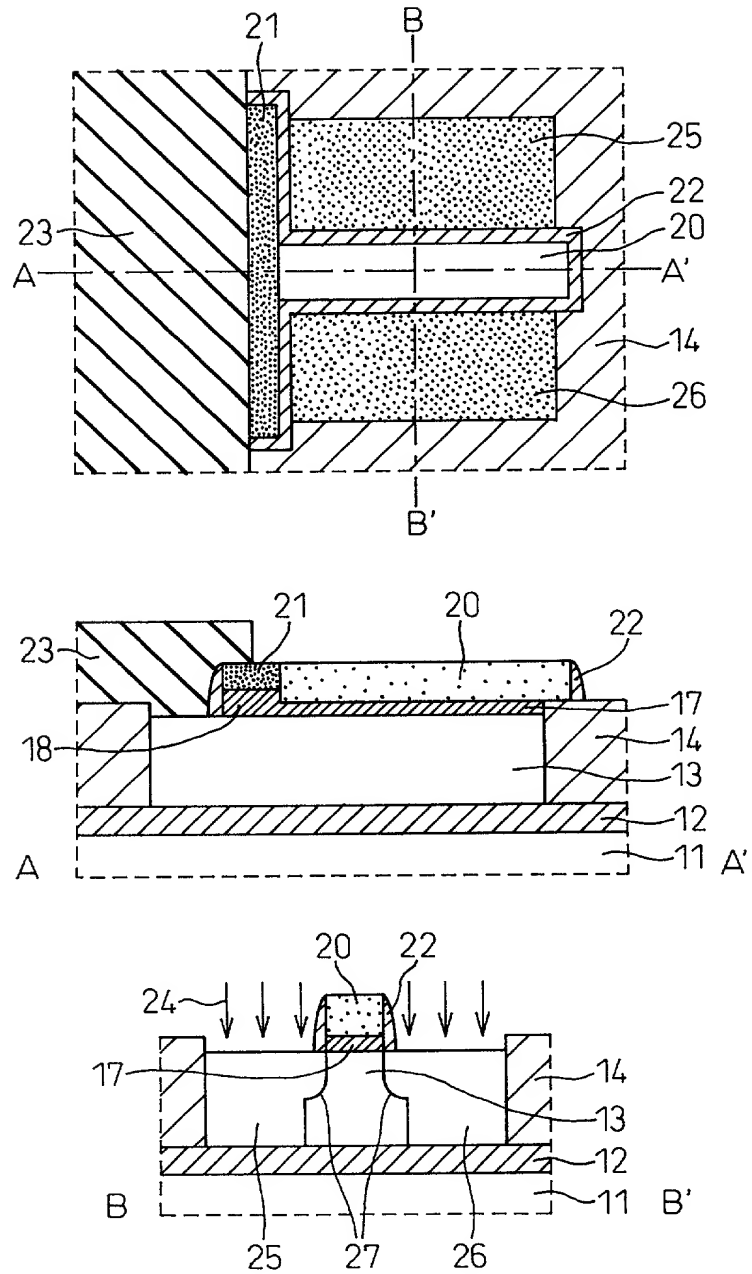


Fig.4 (e)





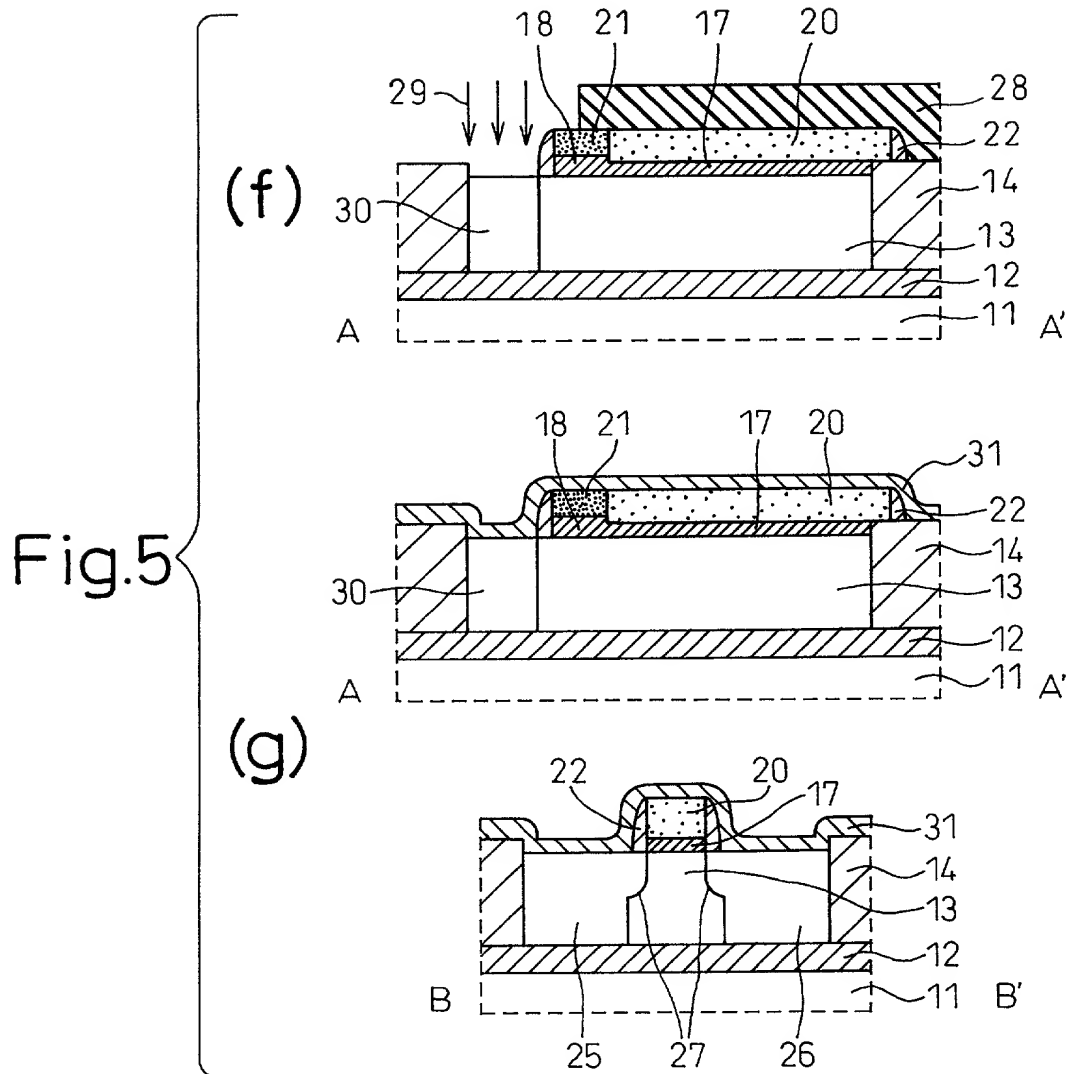
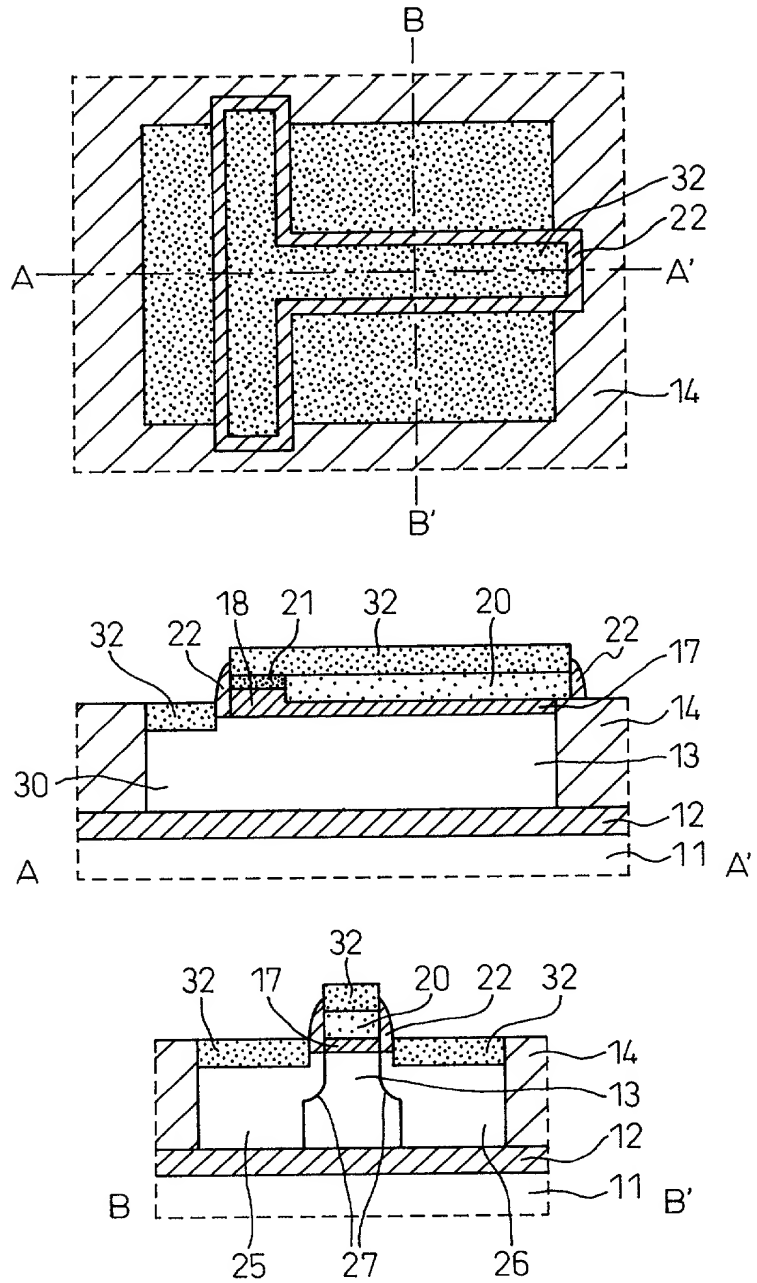


Fig.6 (h)



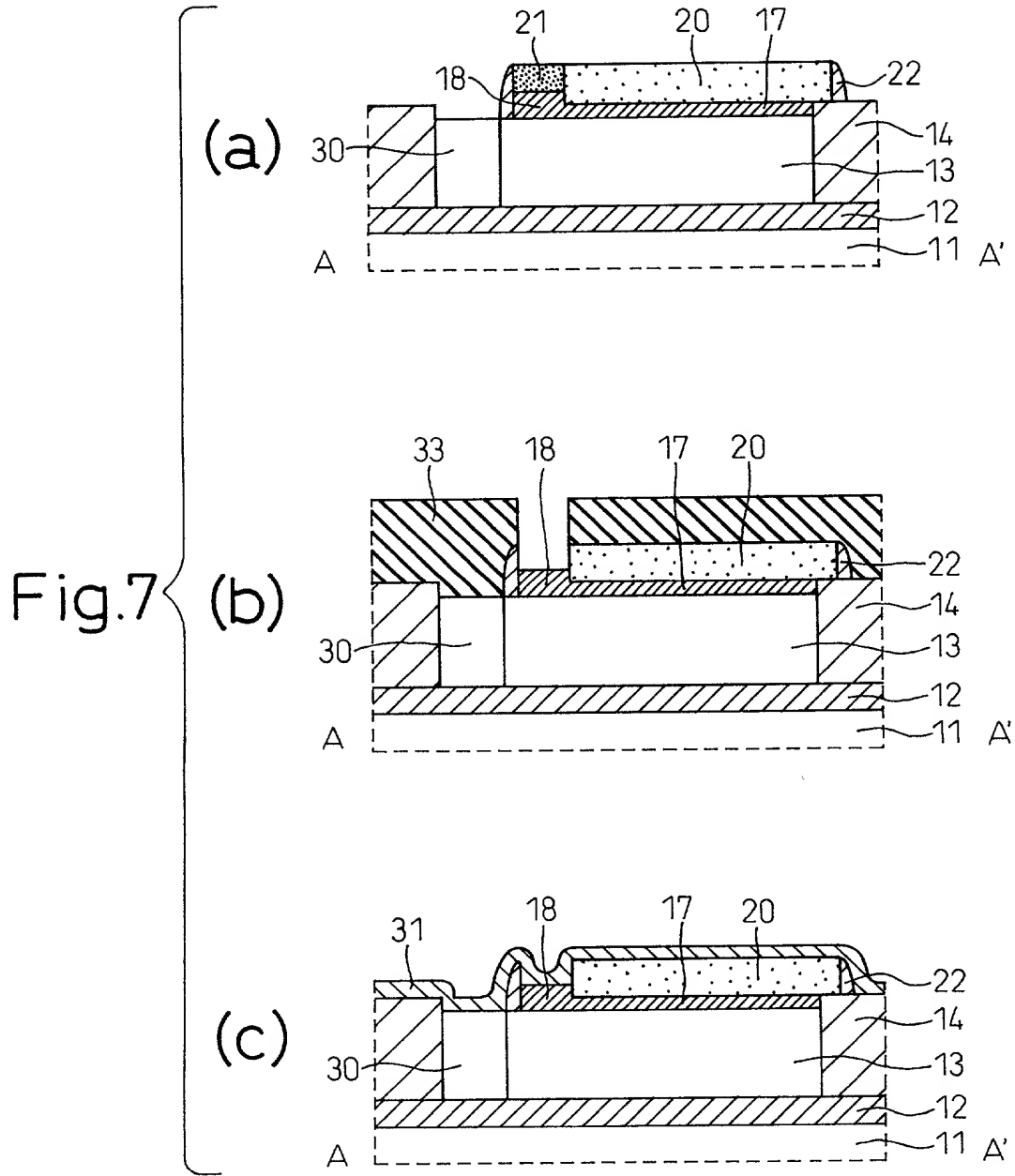
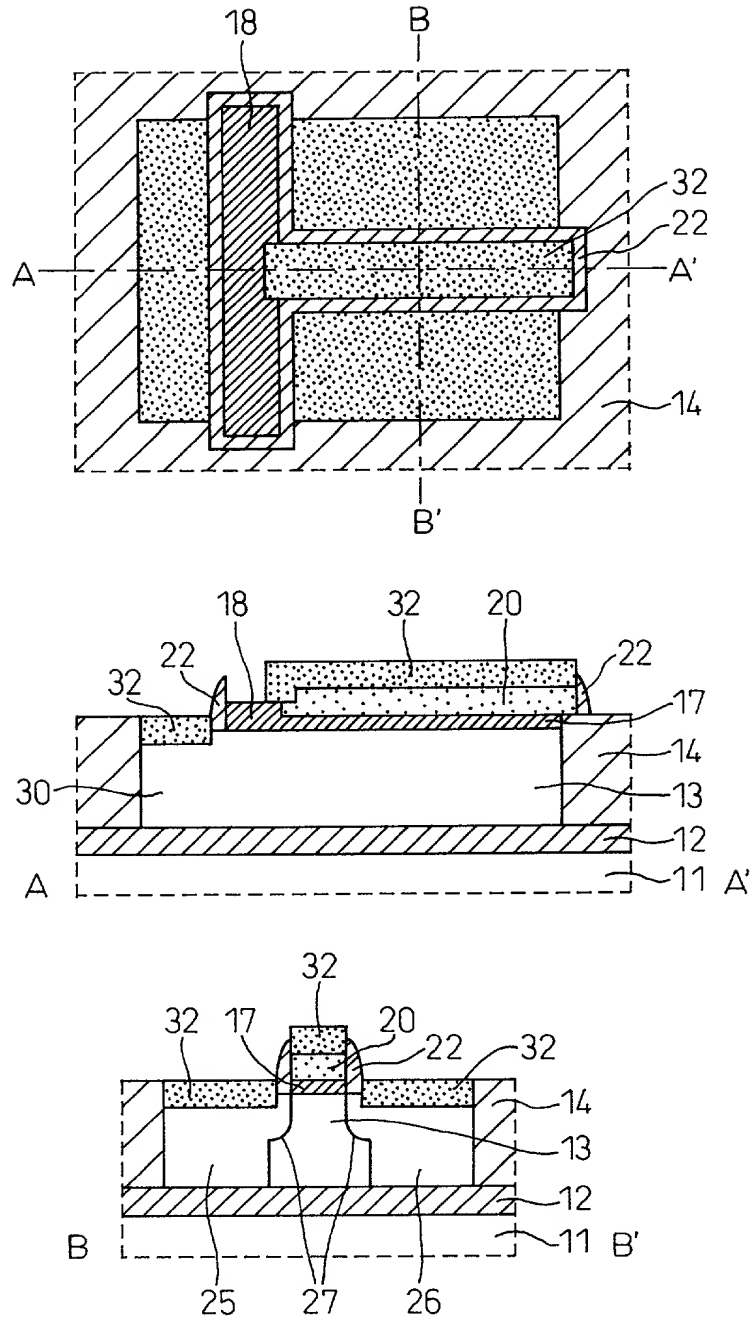
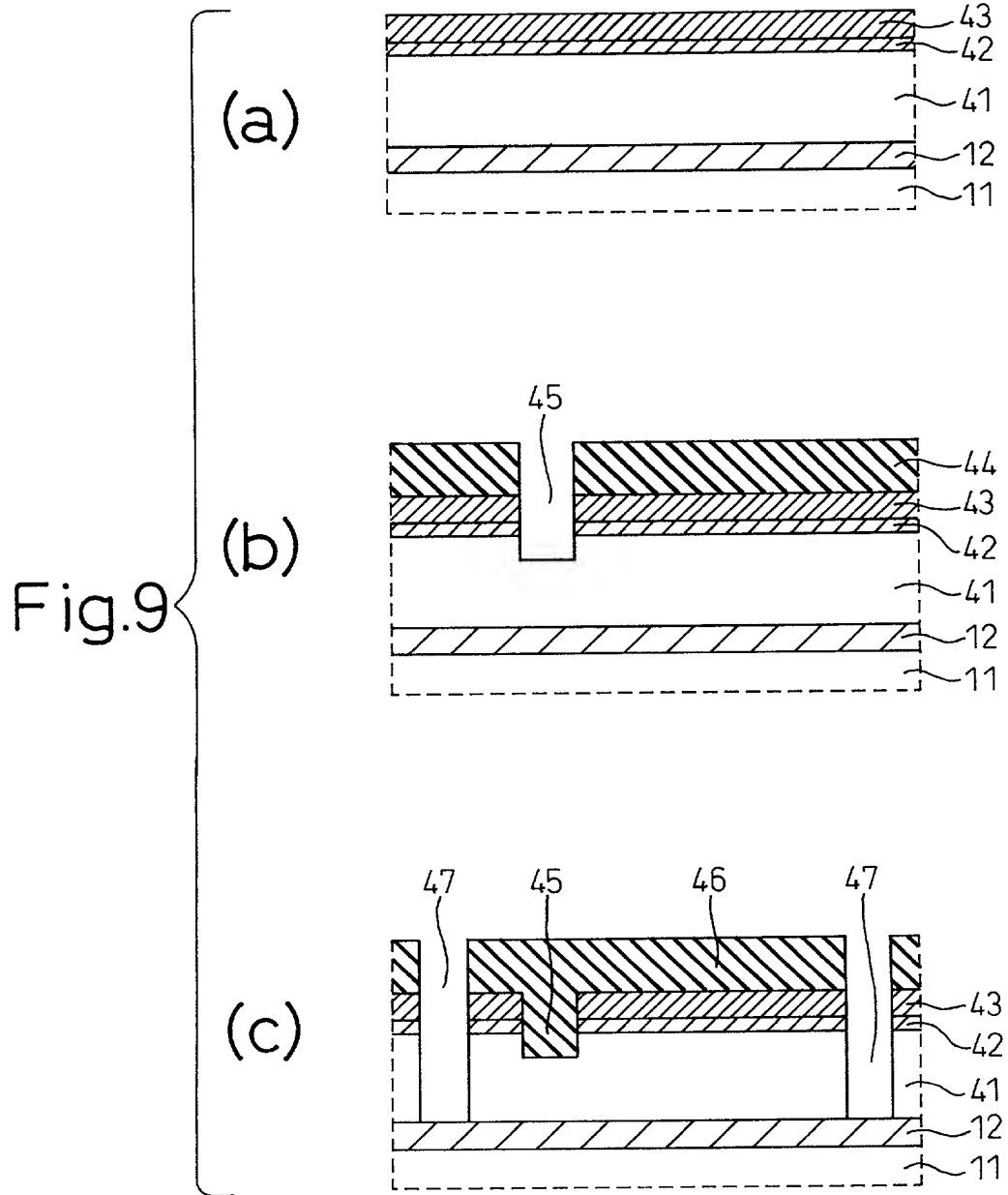


Fig.8 (d)





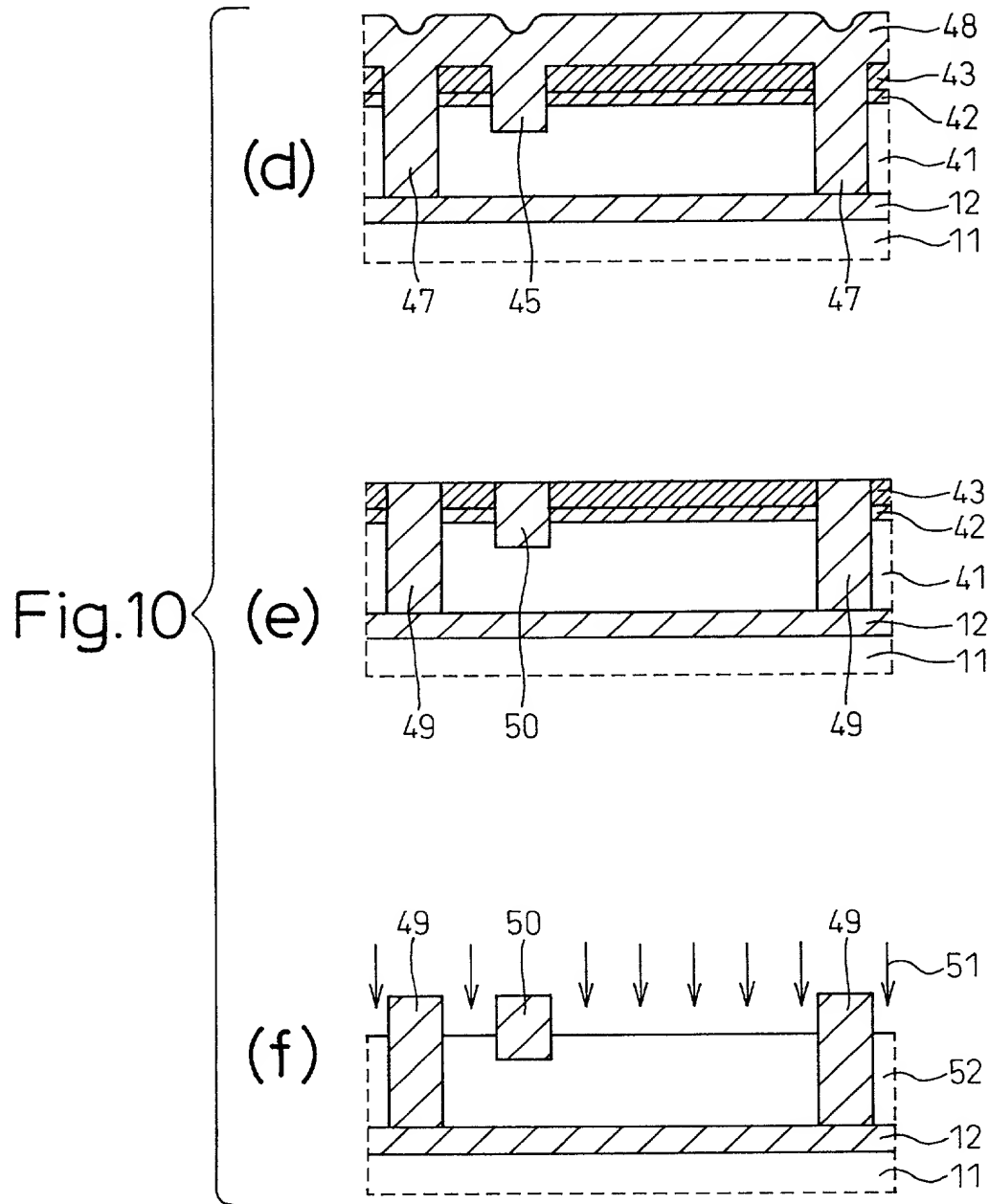


Fig.11

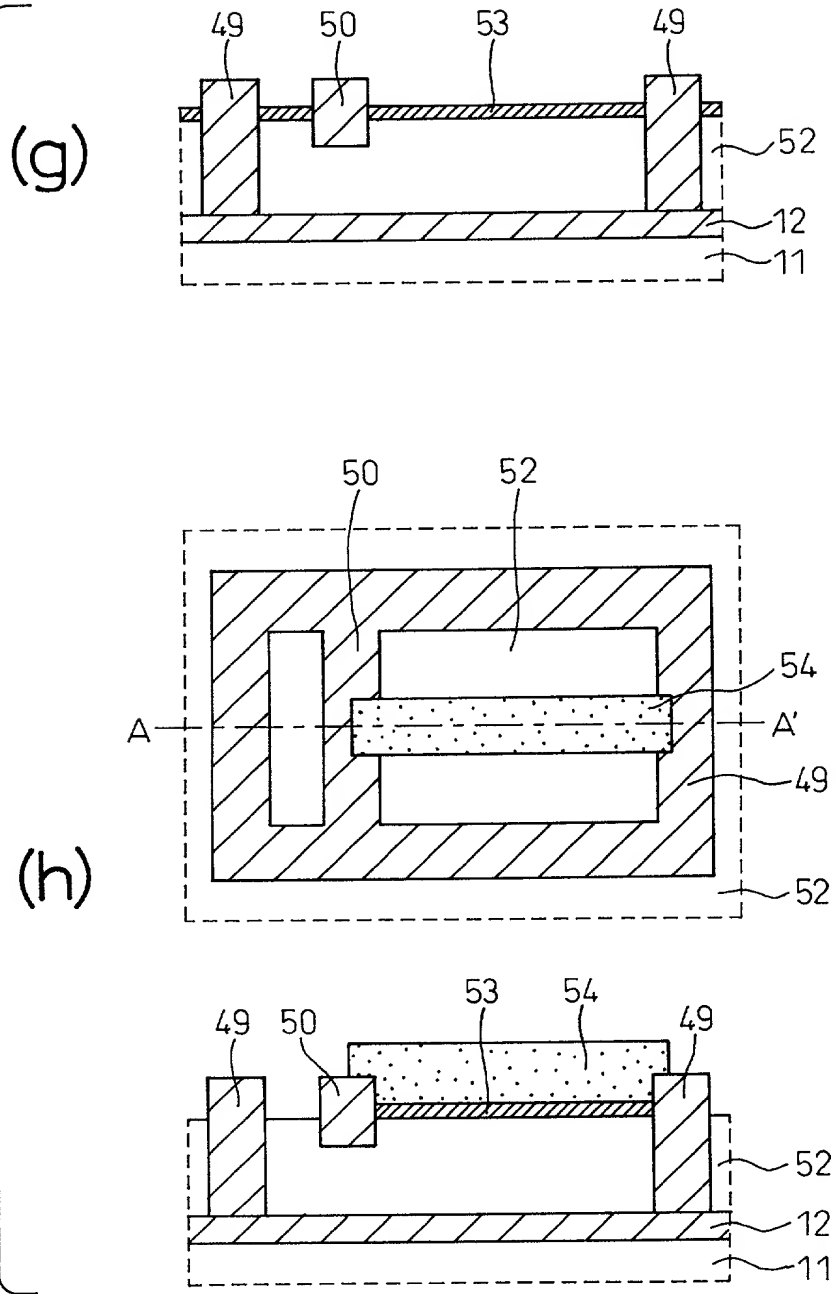


Fig.12 (i)

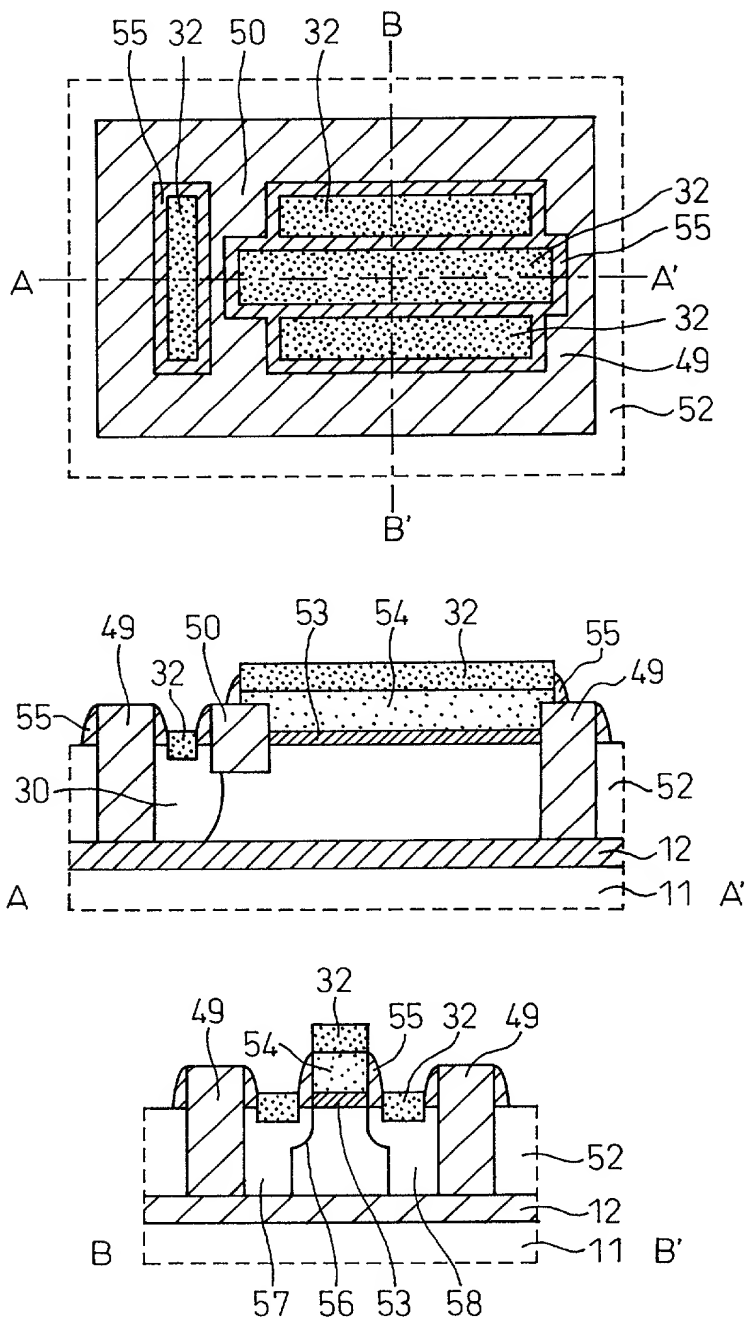




Fig.13

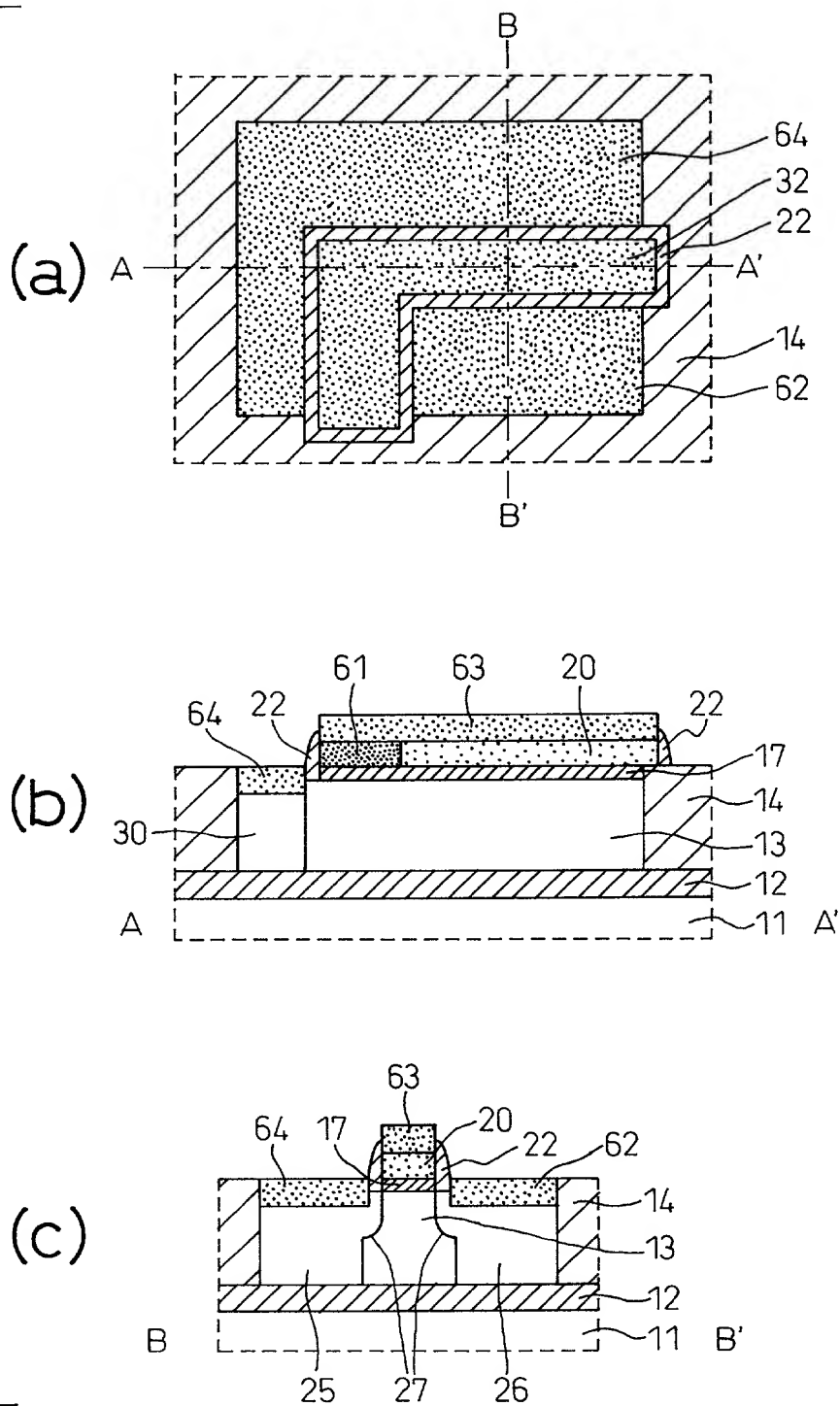
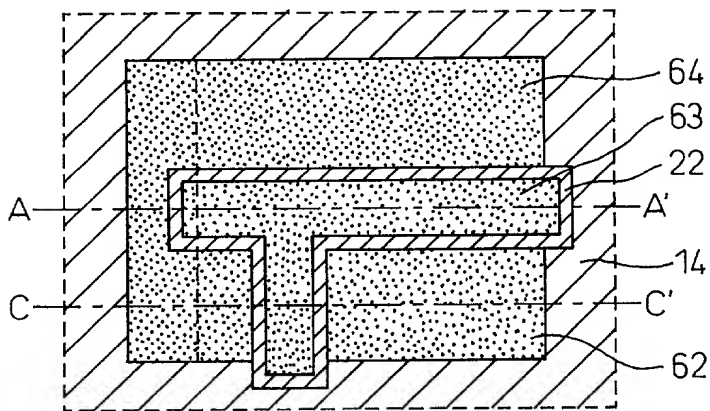
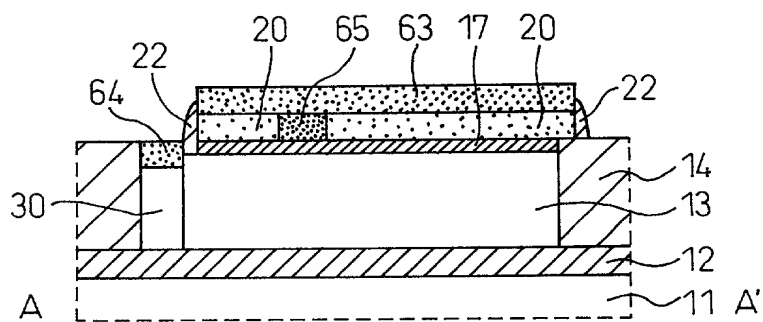


Fig.14

(a)



(b)



(c)

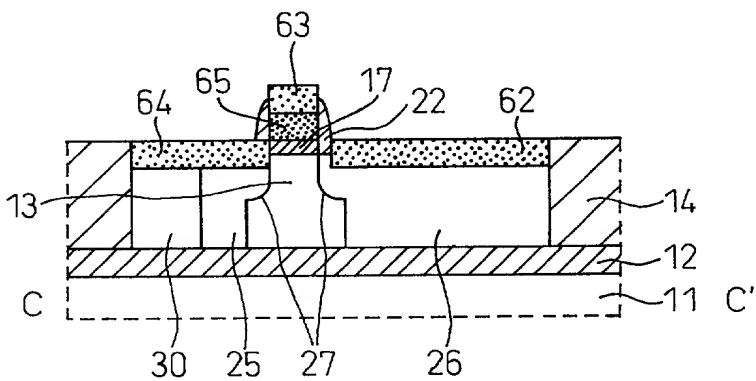


Fig.15

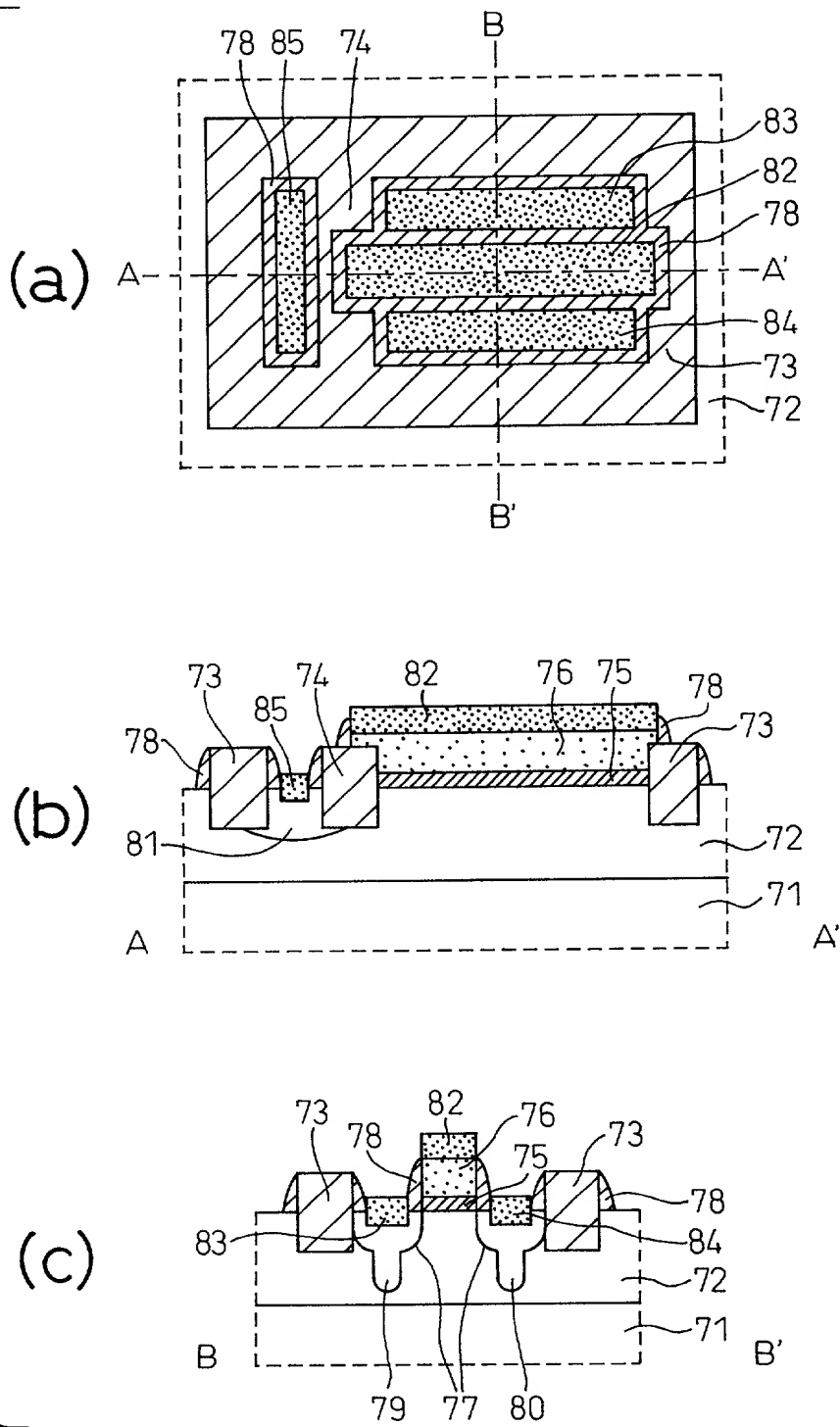
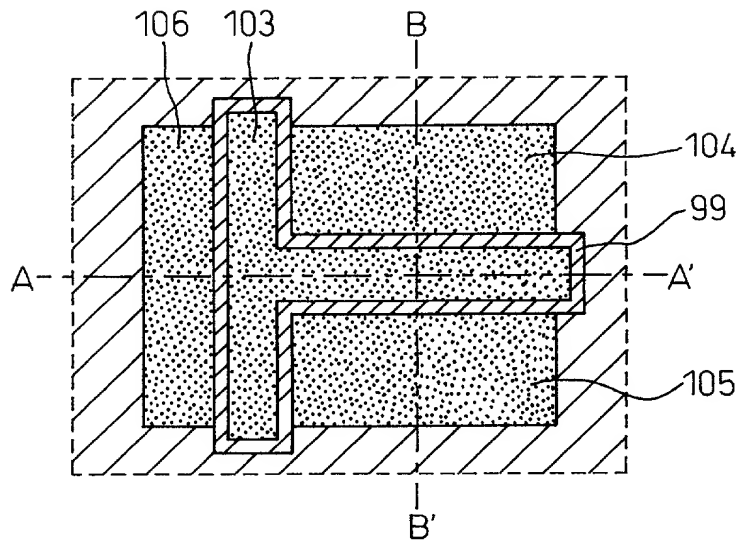
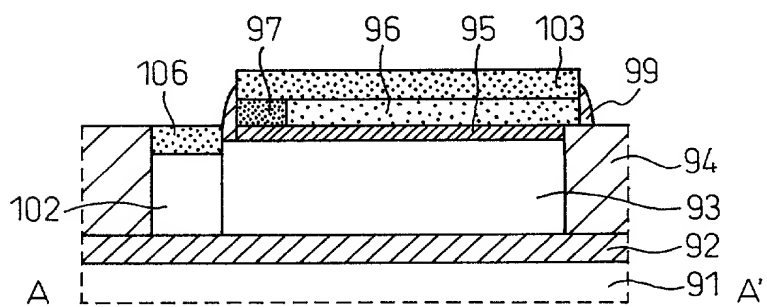


Fig.16

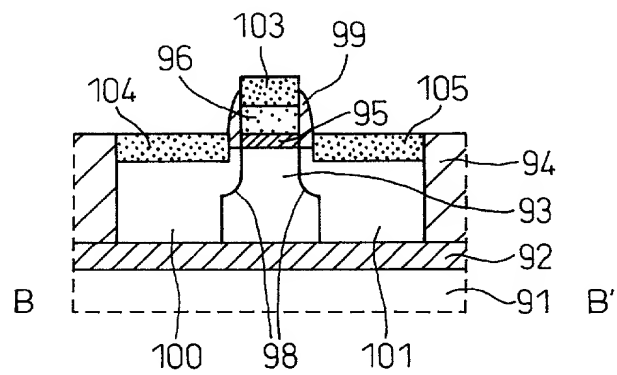
(a)



(b)



(c)



**Declaration and Power of Attorney for U.S. Patent Application**

特許出願宣言書及び委任状

**Japanese Language Declaration**

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

INSULATED GATE TYPE SEMICONDUCTOR DEVICE  
AND METHOD FOR FABRICATING SAME

上記発明の明細書（下記の欄でx印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ \_\_\_\_月\_\_日に提出され、米国出願番号または特許協定条約国際出願番号を\_\_\_\_とし、  
（該当する場合）\_\_\_\_に訂正されました。☐ was filed on \_\_\_\_\_  
as United States Application Number or  
PCT International Application Number  
\_\_\_\_\_ and was amended on  
\_\_\_\_\_ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されたとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

## Japanese Language Declaration (日本語宣言書)

私は、米国法典第35編119条(a)-(d)項又は365条(b)項に基づき下記の、米国外の国の少なくとも一カ国を指定している特許協力条約365(a)項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

### Prior Foreign Application(s)

外国での先行出願

<u>2000-029928(Pat.Appln.)</u>	<u>Japan</u>
(Number)	(Country)
(番号)	(国名)

_____ (Number) (番号)	_____ (Country) (国名)
---------------------------	----------------------------

私と、第35編米国法典119条(e)項に基づいて下記の米国外の特許出願規定に記載された権利をここに主張いたします。

_____ (Application No.) (出願番号)	_____ (Filing Date) (出願日)
--------------------------------------	---------------------------------

私は、下記の米国法典第35編120条に基づいて下記の米国外の特許出願に記載された権利、又は米国外を指定している特許協力条約365条(c)に基づき権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国外の特許出願に開示されていない限り、その先行米国外出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

_____ (Application No.) (出願番号)	_____ (Filing Date) (出願日)
--------------------------------------	---------------------------------

_____ (Application No.) (出願番号)	_____ (Filing Date) (出願日)
--------------------------------------	---------------------------------

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じていることに基づき表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の表明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Priority Not Claimed

優先権主張なし

<u>8/February/2000</u>	<input type="checkbox"/>
(Day/Month/Year Filed)	
(出願年月日)	

_____ (Day/Month/Year Filed)	<input type="checkbox"/>
(出願年月日)	

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

_____ (Application No.) (出願番号)	_____ (Filing Date) (出願日)
--------------------------------------	---------------------------------

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

_____ (Status: Patented, Pending, Abandoned) (現況: 特許許可済、係属中、放棄済)
--

_____ (Status: Patented, Pending, Abandoned) (現況: 特許許可済、係属中、放棄済)
--

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration  
(日本語宣言書)

委任状: 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。(弁理士、または代理人の氏名及び登録番号を明記のこと)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number)  
See list of attorneys and/or agents on page 5.

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第二共同発明者	日付	Second inventor's signature <i>Sadanori Akiya</i>	Date November 13, 2000
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国籍	Citizenship Japanese		
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(第三以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for third and subsequent joint inventors.)

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		<i>Hisashi Watanabe</i>	November 13, 2000
住所	Residence		
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国籍	Citizenship		
	Japanese		
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住所	Residence		
国籍	Citizenship		
私書箱	Post Office Address		
第六共同発明者		Full name of sixth joint inventor, if any	
第六発明者の署名	日付	Sixth inventor's signature	Date
住所	Residence		
国籍	Citizenship		
私書箱	Post Office Address		



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